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54 Production control system, especially for garment manufacture.

57 A production control system is provided, especially for use in a works environment, in which a microsequencer controlled by a Z80 microcomputer board (MUXC) performs continuous high-speed scanning of a multiplicity of operator input devices (OIDs) located at the work stations of individual human operatives. The microsequencer is essentially a single-level pipelined microprocessor communicating with the OIDs via channels and sub-channels, each OID being connected to a respective sub-channel by a single twisted-pair cable. The cable lines are maintained at 24 volts d.c. to supply power to the OID, and the OID, which has a card-reader for reading bar code on cards or tickets passed through it by the operative, transmits data to its sub-channel, and hence the microprocessor, over the same cable by shorting out the two cable lines for short and long pulse periods. The microsequencer checks the validity of each read and responds to the OID to indicate a good read or otherwise - this response is sent in a morse-type code to audio and visual responders in the OID by temporarily reversing the polarity of the same two lines of the communicating cable. The Z80 microcomputer loads microcode into the microsequencer and thereafter supervises the scanning and data-reception and checking functions. Good reads are stored in short-term storage in the MUXC and can be transmitted to up-date the data base of a host minicomputer. Serial link

communication between the MUXC and the host computer is via channels incorporating adapters having optical isolating devices to ensure compatibility and satisfactory transmission over distances in a factory environment.

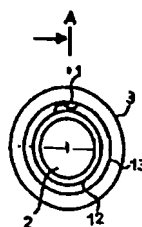


FIG. 4

PRODUCTION CONTROL SYSTEM, ESPECIALLY FOR
GARMENT MANUFACTURE

This invention relates to a production control system for on-line control of factory operations and, in particular but not exclusively, to the control of various functions in a garment manufacturing factory.

5 In today's operating conditions, clothing manufacturers need to maintain tight controls over both factory costs and their investment in stocks and work-in-progress, if their business is to survive. Whilst clothing companies have generally become much more complex to organise and operate over recent years, the tools provided to assist
10 management and supervision in the control of factory operations have not changed dramatically.

One object therefor of the production control system disclosed herein is to provide real-time control of major functions in a garment manufacturing factory, such as production planning, production
15 scheduling, factory loading, factory progress control, section/line balancing, work-in-progress level control, and gross payroll and labour cost control. Whilst existing systems report historically on what happened in the factory yesterday, the aim of the on-line production control system now to be disclosed herein is to achieve
20 up-to-the-minute control of manufacturing operations so that corrective action can be taken to prevent potential problems occurring in the future.

According to one aspect of the present invention there is provided a production or work control system for a works environment, comprising
25 a multiplicity of operator input devices (OIDs) situated at the work stations of human operatives and each having a card reader; and a

multiplexor/concentrator consisting of the combination of a micro-computer and a microprocessor, the microprocessor comprising a micro-sequencer repeatedly scanning the OIDs in a continuous operation to acquire data therefrom which is passed to the microcomputer, the
5 microcomputer carrying out validity checking on the data input from the OIDs by the microsequencer, storing good data in short-term store and returning to the microsequencer signals indicative of the validity or otherwise of each data input consequent upon a card reading at an OID, the microsequencer returning to the individual OIDs the signals
10 indicative of the validity or otherwise of their data inputs, and the microcomputer having input and output ports for communication with a host computer, such as a minicomputer.

The microprocessor/microsequencer may be a bipolar bit-slice microprocessor of the single-level pipelined type driven by writeable
15 microcode. The microcomputer may be a Z80 computer board.

According to another aspect of the invention there is provided an operator input device (OID) for use in a system of production or work control, comprising a card reader for scanning a card or ticket bearing encoded data when said card is placed in the card reader and
20 generating electrical signals representative of said encoded data, a cable for supplying low-voltage external electrical power to the OID over a pair of electrical lines, pulse train-generating-circuitry responsive to the card reader output signals to derive a stream of pulses of at least two different durations representing the encoded
25 data, said pulse train-generating-circuitry taking its electrical

supply from said pair of lines, and short-circuiting means powered from said pair of lines and responsive to said stream of pulses to substantially short together said lines for a succession of time periods corresponding to the time durations of said pulses, whereby
5 the data from the card or ticket is transmitted by the OID on the same cable pair as supplies the OID with its electrical power.

The short-circuiting means may be driven by an optical isolator having a radiation emitter to which said stream of pulses is applied, and a receiver responsive to the radiation from said emitter and
10 electrically isolated therefrom, such as by diodes.

In the preferred embodiment, each card or ticket bears two parallel bar code tracks, the first being a clock track of regularly spaced thin bars, and the second a data track having either a thick bar or a space opposite each thin bar bit of the clock track to
15 indicate 'ones' and 'zeros', and the scanning means comprises a first emitter/receiver combination scanning the clock track and a second emitter/receiver combination scanning the data track. The OID includes two monostable circuits having different time periods to generate pulses of different widths, and logic circuitry responsive
20 to the signals from the receivers of the scanning emitter/receivers to direct each clock bit to the triggering input of one or other of the monostable circuits according to whether the data track is simultaneously showing a bar or a space. The outputs of the two monostable circuits are gated together to provide the stream of pulses
25 that is applied to the transistor feeding the light-emitting diode of

the optical isolator. The OID further comprises audio and/or visual response means which is energized by the external power supply cable when the polarity of the voltage on the cable line pair is reversed.

According to a further aspect, communication between the MUXC
5 and a host minicomputer is established over a serial link including optical isolating devices. Power is transferred via a transformer.

The system can load the factory with an optimum style mix to maintain targetted production levels, whilst meeting customer delivery requirements. The level of work-in-progress can be maintained at the
10 level required for efficient factory operation, and production orders can be systematically progressed so that they emerge completed into the warehouse in the minimum throughput time.

Much of the hardware used in the system to be described has been designed and built specifically for the needs of the clothing industry,
15 but such hardware may be used in many other industries, particularly the OID as a means of inputting information relating to the human operative, his particular task and the operation to be performed in a computer processor (CPU).

An OID is mounted at each human operative's workplace and is used
20 to read bar-coded operator cards, operation cards, and bundle cards submitted by the operative.

Each OID is connected to a data concentrator or multiplexor (MPX), which is microcomputer controlled. The MPX performs certain checks on data fed in from the OID's, and then transmits the data
25 for processing to the central computer system, which may comprise a

minicomputer system, e.g. a Hewlett-Packard HP1000, with central processor, disk drive, visual display unit(s), printer and optional magnetic tape back-up.

Each human supervisor may have a terminal comprising a small
5 visual display unit, which is connected to the central computer system and is used to input information to, or request data from, the computer.

The OID enables each operative to clock in and out, at the beginning and end of a day, thereby eliminating time wasting at
10 traditional clocking stations. The operative also uses the device to notify the central computer of the operation currently being carried out and what job lot is currently being worked on. This enables the central computer to calculate gross payroll, fully automatically. The operative uses three kinds of card, a personal
15 card with which he/she clocks in and out, an operation card, with which he/she indicates the operation he/she is performing, and a job lot card, which travels with each job lot through the factory and indicates on which job lot the operative is working.

The supervisor terminal, which is of the television type, has a
20 keyboard by means of which the supervisor can call up information as to how much work each operative has done that day and at what rate he/she is working, also information as to where each job lot is in the factory, and information on how much work is waiting at each operator station, to enable the supervisor to balance the work flow
25 through the factory much better. Also, on the screen, he/she can

obtain accounting reports showing all off-standard work and operator down-time on his/her section, by operative, by time and by cost.

The whole system is real time, which means that any time a supervisor enquires for information it is up to date.

- 5 The system also allows for a whole series of problem types to trigger warning signals at the supervisor's terminal, such as production at a certain operation falling below the minimum rate per hour or a particular machine being broken down for more than a certain time or the pile of work at any particular station rising above a
- 10 critical level.

Arrangements according to the invention will now be described by way of example and with reference to the accompanying drawings, in which:-

Figure 1 is a pictorial view of an Operator Input Device with a
5 card reader,

Figures 2A and 2B are a circuit diagram of the Operator Input Device,

Figure 3 shows a bar-coded card of the type to be read by the card reader of the Operator Input Device,

10 Figure 4 is a diagram showing an arrangement of emitters and receivers for scanning a card in the card reader,

Figures 5A and 5B are a circuit diagram of a microsequencer for scanning Operator Input Devices and receiving and responding to data inputs therefrom,

15 Figure 6 is a circuit diagram of one of eight channels whereby the microsequencer communicates with the Operator Input Devices,

Figure 7 is a circuit diagram of one of a multiplicity of sub-channels whereby each channel as shown in Figure 6 can communicate with a group of Operator Input Devices,

20 Figures 8A to 8J are circuit diagrams of blocks of a Z80 micro-computer board which has overall control of the microsequencer of Figures 5A and 5B and interfaces with a host minicomputer,

Figure 9 is a circuit diagram of isolating adapter circuitry whereby the Z80 microcomputer of Figures 8A to 8J interfaces with the
25 host minicomputer, and

Figures 10A and 10B are timing diagrams for the channels and sub-channels of Figures 6 and 7.

Operator Input Device (OID)

The operator input device is driven from a multiplexor concentrator

5 MUXC. The device reads optical bar-code produced elsewhere by software driving a standard HP2631B printer. The OID reads a bar data and clock track and sends the results to a MUXC. The MUXC communicates back the status of the read to the OID which in turn, by an audio/visual response, communicates to the operative.

10 Multiplexor/Concentrator (MUXC)

This device comprises two microprocessors (a microsequencer or bit slicer and a Z80 Computer board). A combination of microcode and firmware allows data from up to 128 OID's to be temporarily stored for up to eight hours in memory as back-up to the data being trans-

15 ferred to an HP1000E central computer where the data is permanently stored and updates a data base. The data base provides information in real-time to terminals on the shop floor.

Communication Channels

The data transfer between the MUXC and the central computer is

20 via isolating adapter circuitry allowing RS423 protocol to interface with RS232 protocol.

Data transfer between the MUXC and the OIDs, and power supply from the MUXC to the OIDs, is by a system of channels and sub-channels.

Software for the above hardware includes the following.

Microsequencer software

Microcode is provided for the microsequencer or bit slicer to enable it to scan the OIDs and respond to the data inputted from the OIDs.

5 Z80 Software

The Z80 software includes a program for loading the microcode into the microsequencer and a main program enabling the Z80 to control the entire operation of the MUXC.

Considering now the operator input device (Figure 1), this appears
10 externally as a box 10 with a side reader 12 presenting a card-reading slot 11, green and red signal lamps 13, 14 in the form of light-emitting diodes being provided on the box front. A single twisted pair cable provides the link between the OID and the MUXC, carrying both data signals between the OID and the MUXC and a 24 volt power
15 supply from the MUXC to the OID. As already indicated, the MUXC can sustain up to 128 OIDs. The OID box 10 contains a single printed circuit board.

There are three data types entered via the OID, they are:

- Employee (Operative) Identification
- 20 - Operation (Work) Identification
- Work Unit (Job Lot) Identification

The OID itself has no ability to operate on the different types but merely detects and sends the detected signals to the MUXC.

When the power is on, the green lamp 13 is lit and stays on
25 constantly showing the OID is in working status. When a card is

passed through the reading slot 11 the data is read and passed to the MUXC where it is checked for three possible states. One of these states is returned to the OID where both an aural signal and a visual signal via the red lamp 14 are emitted.

5 The three states returnable to the OID are:-

1. Good Read

If the read is accepted without physical or logical error then a single aural tone and a single red lamp pulse are caused to be emitted from the OID. The operative can then return to his/her work.

10 2. Good Read but Logical Error

The system is designed so that an operative (employee) identification and the type of work (operation) must have been input in that order before any work (job lot) ticket can be passed through the reader and be accepted, i.e.

15

20

EVENT	SEQUENCE							
	A		B		C		D	
EMPLOYEE	/	1	X	2	/	1	X	3
OPERATION	/	2	X	1	X	3	/	2
WORK TKT	/	3	/	3	X	2	X	1

Any sequence other than 'A' will invalidate work ticket transactions thus preventing the operative from receiving a correct input good read as in (1) above. The red lamp and the aural bleeper will then return a series of six alternate long and short pulses to enable the operative to distinguish between a logical and a physical error.

25

3. Physical Error

A physical error is caused by a misread of the characteristics on the input card (any type). This may be caused by damage to the card, incorrect method of slotting the card through the reader or
5 malfunction of the OID, though this latter is designed such that should it physically malfunction the green lamp 13 will be extinguished. In case of a physical error, a series of eight short regular pulses will be given by the aural bleeper and the red lamp.

When the OID reads a bar-coded card, the black to white contrast
10 ratio on the bar card is detected by infra red detectors and converted to digital pulses of the correct width. Depending on the bar card read, the MUXC will respond back to the OID by sending a coded tone to identify a good read, or a physical or logical error.

The MUXC channel to which the OID is connected holds one line A at
15 +12 volts through a 120 ohm resistor and the other line B at -12 volts through another 120 ohm resistor. This is the normal state of the circuit; when the MUXC channel wishes to acknowledge some form of read, the polarity is reversed which energises the audible bleeper and lamp in the OID. The standing current is about 20 mA so that a
20 voltage of about 18 volts is available at the OID terminals. The OID itself generates signals by shorting the lines together for very short periods. A zero bit is indicated by a 100 microsecond pulse and a one bit by a 300 microsecond pulse. In fact, the lines are pulled to within about 4 volts of each other rather than a dead short.

25 Referring to Figures 1A and 1B, the OID circuit is as follows.

The voltage applied across input terminals 15 (line A) and 16 (line B) is applied via line-isolating diodes 17 to a reservoir capacitor 18 which charges to about 16 volts (line less 2 diode drops). This supplies a 12 volt regulator 19 which powers the rest of the circuit, except for the audio unit 20 and red lamp 14 which during normal voltage on the terminals 15, 16 are isolated by diodes 21. A series chain includes a brightness-adjustment resistor 22 and three LED's, one of which is the green (ready) lamp 12 while the other two are infra-red LED's 23 which illuminate the clock and data tracks on the cards to be read. The data and clock tracks on a card, illuminated by respective LED's 23, are read by respective photo-transistors 26 the outputs of which are fed to respective identical circuits 24, 25. Each of the circuits 24, 25 comprises a cascode 27 and a MOSFET operational amplifier buffer 28. A resistor chain 29 provides bias to the cascodes and operational amplifiers of both circuits 24, 25. The operational amplifiers 28 have a high output for black bars on the card being read.

The durations of the output bits of the OID are determined by a 300 microsecond monostable circuit 31 (one bit) and a 100 microsecond monostable circuit 32 (zero bit). By means of a three-gate logic circuit 30 the clock track signal output of the circuit 25 is switched by the data track signal output of the circuit 24 either to the monostable 31 to generate a one bit (data black) or to the monostable 32 to generate a zero bit (data white). White-to-black transitions on the clock track thereby trigger one or other of the monostables 31, 32.

The outputs of both monostables are combined into a single pulse train at an OR gate 33, the output of which is applied to the base of a drive transistor 34 which drives an opto-isolator 35. The opto-isolator 35 consists of a photo-diode 36, in series with the transistor 34, and a photo-transistor 37. An output transistor 38 in Darlington connection with the photo-transistor 37 effectively shorts the lines 39, 40 via isolating diodes 41 and damping resistors 42.

Line polarity reversal at the terminals 15, 16 by the MUXC energises the audio bleeper 20, and also the lamp 14 in parallel with it, via the diodes 21, the remainder of the OID circuit then being isolated by the diodes 17.

Figure 3 shows a typical bar-coded card 43 to be read by the OPI. The clock track 44 and the data track 45 are immediately one below the other, the clock track consisting of a horizontal series of evenly spaced thin vertical bars while the data track consists of thick bars irregularly spaced. The clock track contains 60 OR-signs and the data track provides a cursor-sign under a corresponding clock pulse where the data bit is a one. The bottom edge 46 of the card is a zero reference, and the data and clock tracks are printed between 4 mm up from the bottom and 17 mm from the bottom. The bar code tracks are printed by the HP2631B printer on comparatively thin white flexible sheet so that each card is in the form of a ticket that can, if it is a job lot card for example, be readily stapled to the work. The cards can be printed on sheet that is a number of cards wide and separated afterwards by guillotining.

Figure 4 shows the scanning arrangement of emitters and receivers in the reader 12 of the OID 10. The zero reference edge 46 of the card 43 rests on the horizontal upper edge 47 of a shim plate 48 in the lower part of the card reader slot 11. The card is moved horizontally through the reader slot 11 from back to front of the reader. The two infra-red LEDs 23 illuminate the clock track 44 and the data track 45, respectively, and the two photo-transistors 26 receive, respectively, the reflections from those tracks. The photo-transistors 26 are angled obliquely in order to provide adequate space, and the clock track 44 and the data track 45 are scanned through respective wedge-form transparent blocks 49, 50 separated by an opaque body 51, further opaque bodies 52, 53 being situated above and below the transparent blocks. The portion 54 of the body of the reader 12 that lies on the side of the slot 11 remote from the emitters 23 and receivers 26 is removable, and is both opaque and non-reflecting.

Referring again to Figure 3, the format for the bar code on each card (starting from the leading end as passed through the reader) is as follows (note each byte is read lowest significant bit first):

1. Four run-in bits: "1010"
 2. One sync byte (ASCII 16hex): "01101000" = eight bits
 3. Four data bytes sent MSbyte/LSbit first = thirtytwo bits
 4. One error correction code (ECC) byte = eight bits
 5. One parity byte = eight bits
- This makes up the total of sixty bits.

The sixteen bits devoted to the parity and EOC bytes for the detection and correction of errors gives good protection of the data having regard to the nature of the cards and the usage to which they are put.

5 As already stated, the multiplexor/concentrator (MUXC) comprises two microprocessors, a Z80 board and a microsequencer. The Z80 computer board controls the entire operation of the network multiplexer and interfaces with the host HP1000E minicomputer via a serial link. The microsequencer is located physically and functionally
10 between the Z80 microprocessor and the operator input devices and is a bipolar bit-slice microprocessor driven by writeable microcode which scans 128 sub-channels in an endless sequence servicing the OIDs and buffering data bidirectionally between them and the Z80. The 128 sub-channels are grouped in fours, with four such groups of four (16 sub-
15 channels) being serviced by each of eight main channel boards that are in turn serviced by the microsequencer.

 The microsequencer (Figures 5A and 5B) is based on Advanced Micro Devices 2900-series integrated circuits. In essence it is a standard AMD 2901 single-level-pipelined microprocessor. The microprogram is
20 organised as a 256 word by 32 bit array and is stored in the first quarter of a 4 x MK4801 (Mostek 70 nanosecond 1k x 8 bit static RAM) memory array 55. A microprogram sequencer 56 is 8 bits wide and consists of two 2909 chips in cascade. Only two sequencing modes are used: either sequential (S0-S1=0) or direct branch (S0-S1=1). The
25 direct branch can be modified by three S-bits in a status register 57

to give an eight-way branch dependent on the state of a sub-channel as received at 86.

The microprogram word is decoded and is latched at the beginning of each clock cycle in various chips 58 - 64. Wherever a microword field is encoded (e.g. four 'data-in' paths encoded into bits 25/24) the decoder chip (e.g. 61) is upstream of the latch (e.g. 62) to increase speed. The microwords designate either a Branch or an ALU (Arithmetic Logic Unit 74) instruction cycle according to the value in a 'data-out' (D-out) field (bits 28-26). If these bits are all ones (indicating a Branch instruction) the microprogram either branches or continues depending on:

- a. whether or not there is at least one status register bit under a 'one' in a mask field (bits 18-8) having the value 'one'. The 11-bit status register is logically AND-ed with the 11-bit mask field and the resulting eleven bits are OR-ed together.
- b. The condition of an R-bit (21). If zero the branch is taken for any 'one' under the mask, otherwise the sense of the branch is reversed.
- c. The condition of an S-bit (20). If 'one' the contents of the S-20 bits in the status register are OR-ed into the branch address to give an eight-way branch.

The branch address is taken from a D-field (7-0) in the micro-instruction. The I-field (ALU instruction) is always zero (NOP) for Branches so that the ALU does not alter any registers etc. The D-in field is immaterial for Branch instructions.

If the D-out field is not all ones an ALU instruction is indicated; however, in this case bit 16 is always 'one'. The corresponding reduction of the I field from nine to eight bits results in a much more convenient arrangement for assigning the
 5 microword bits. If the I-field designates input from the D-inputs this is obtained from one of four sources as indicated by the D-in field (bits 25, 24). These are:

- 0 - data field in microinstruction (bits 7-0)
- 10 1 - Z80 Computer Parallel output (i.e. microsequencer input from controlling computer)
- 2 - Data RAM 73 with ALU 74 carry-in zero
- 3 - Data RAM with ALU Carry-in zero for a timer cycle, one otherwise.

Near the end of the microcycle ($t=200$ nsec) the ALU 74 output is
 15 strobed into the destination designated by the D-out field as follows.

- 0 - None
- 1 - Data Ram 73
- 2 - Z80 Parallel input (i.e. microsequencer output to controlling computer)
- 20 3 - Low-order RAM address register 65
- 4 - High-order RAM address register 66
- 5 - Low-order RAM address AND external (E) register 67 outputting to the channels and sub-channels
- 6 - E register 67 alone
- 25 (7) - (Branch instruction)

The high-order three bits (31-29) of the microinstruction are latched in a 'Scope Trigger' register 68. This is for diagnostic trace purposes only.

The clock is a standard 8MHz oscillator 69 followed by a binary
5 divider 70 producing a 4MHz square-wave (the basic clock pulse). This feeds a delay line 71 with five 50 nanosecond taps, and decoders 72 produce three subsidiary clock pulses. With reference to the basic clock (CP) rising at $t=0$ and falling at $t=250$, these subsidiary clocks are as follows:

10 OA - rises 0, falls 25. Disables the Data-in paths momentarily to avoid bus contention.

OB - falls 150, rises 200. Activates Data RAM write enable pin.

OC - rises 200, falls 250. Clocks Data-out registers.

All clock signals are disabled when bit 7 of the Z80 output port
15 PIOC is 'one'.

A timer 75 is a free-running LM555 oscillator operating at about 16Hz. It is synchronised with the microsequencer scan by a circuit 76 and the microprogram so that the T-stat is 'one' for exactly one complete cycle every 1/16th of a second.

20 During the microcode initialisation cycle a register 77 is connected to the address lines of the microcode array and four registers 78 (32 bits) to the data lines. Z80 software loads each of the five registers for each microword, finally strobing the array write line to write the word into the array. Ports A and B (Z80 computer) are
25 the data and control/address ports for this operation. After

microcode load bit 6 of port B is set zero which disconnects the above arrangement and establishes the normal pipelined data flow. Subsequently bit 7 of Port B is set zero which enables the clock pulses. A circuit 79 ensures that the microprogram starts cleanly at
5 address zero.

In normal operation the port 81 addresses register 80 via register 85 for the routing in of Z80 data from port A. Register 82 is used in the routing of data out to Z80. Monostables 83 and 84 provide A and B strobe pulses for the timing of port A handshakes which are
10 bidirectional.

A listing of the microcode for the microsequencer of Figures 5A and 5B is appended to this specification as Appendix I.

The program operates in an endless cycle scanning sub-channels 0 to 127 decimal. The board contains an eight byte work area for each
15 sub-channel and this is initially formatted by the reset function. Each work area contains the current state, the current time-out value and the current byte and bit count for the sub-channel. All slots are initialised to

State - 0
20 Time-out - 15
Byte (cell) - 2
Bit - 0

The cycle starts at location zero.

If the reset line (from Z80) is true a branch is taken to the
25 reset routine.

The sub-channel counter is incremented and the clock line (to channels) is activated. (If the sub-channel is zero this pulse is extended and the T-stat is set if this is a timer cycle).

The state of the sub-channel is used to give an immediate branch
5 to the entry point in the microcode for the current state.

The sub-channels move individually through the states as follows.

State 0 - Idle:

Enter from reset. Leave to state 1 on OID request.

State 1 - Reading for SYN character:

10 Enter from state 0. Leave to State 2 on detecting SYN
character. Leave to state 3 on time-out.

State 2 - Reading data:

Enter from state 1. Leave to state 3 on receiving last
data bit or on time-out.

15 State 3 - Ready for transfer to Z80:

Enter from states 1 or 2. Leave to state 4 when
Microsequencer - Z80 path is free.

State 4 - Transferring data to Z80:

20 Enter from state 3. Leave to state 5 when nine bytes
(sub-channel address and eight byte work area) have been
transferred.

State 5 - Waiting for acknowledgement from Z80:

25 Enter from state 4. Leave to state 6 when Z80 has sent
back the acknowledge code and morse code signal has
been built in the work area.

State 6 - Acknowledging to OID.

Enter from state 5. Every timer cycle the next bit of the morse code is played out to the OID. Leave to state 7 when all the code bits have been sent.

- 5 State 7 - Enter from state 6. Leave to state 0 after selectively resetting the sub-channel work area.

Note: States 4 and 5 are exclusive to a single sub-channel at a time. All other states are shareable.

Figure 6 shows the circuit of one of the eight channel boards
10 that serve as interfaces between the microsequencer of Figures 5A and 5B and the Operator Input Devices (via the sub-channels). Each channel has its own unique channel address (bits 0-7), set on switches on the board, and can support up to sixteen sub-channels. Each sub-channel in turn supports one OID.

- 15 The microsequencer controls the channel timing (Figures 10A and 10B) via a backplane line (SYSCK/EC) inputting to the channel at 116. The microprogram causes this line to carry a stream of pulses each one occurring at the start of a sub-channel period. At the start of sub-channel zero's period this pulse, normally 750 nsec, is extended to
20 1500 nsec. Each full cycle is 128 sub-channels in length.

At the trailing edge of each clock pulse a monostable 88 is fired producing a pulse of approx 150 nsec which is passed down a delay line 89 with 100 nsec taps. The original pulse and the first three delayed pulses are denoted T0, T1, T2 and T3 respectively. A second
25 monostable 90 (period 1100 nsec) is fired by the leading edge of the

clock pulse and a seven-bit counter 91, 92, clocked at T0, is cleared if this monostable has timed-out and incremented if it has not. The effect is that the counters on all channels keep in step with the microsequencer.

5 The high-order three bits of the seven-bit counter are compared in a comparator 93 with the address set by the address switches 94. An equal condition means that this channel is selected and this activates the sub-channel decoder 95, 96. The same signal is ANDed at 97 with T3 to provide the 'Channel Clear' (CHCLR) signal at 98.

10 The sub-channel decoder 95, 96 drives one line per sub-channel to select the sub-channel according to the low-order four bits of the counter 91, 92.

 The basic sub-channel circuit is shown in Figure 7. Line driver circuit 99 is simply a bilateral switch which in the normal condition
15 (input low) holds line A to plus twelve volts via a 120 ohm resistor and line B to minus twelve volts via a 120 ohm resistor. Thus normally line A is positive and line B negative and, due to the OID standing current of about 20mA, the actual voltages are about plus/minus 9 volts.

20 An operational amplifier 100 senses the line pair using a balanced differential input network 101 and its output, after clamping and filtering at 102, is logic zero at input 103 to a monostable 104, in the normal line state.

 The OID signals a '0' bit by a 100 microsec shorting pulse on the
25 lines and a '1' bit by a 300 microsec pulse. At the leading edge of

this pulse the monostable 104 is fired for its period of 200 microsec. At time T0 flip-flops 105 and 106 are clocked, and at time T1 they contain 0 and 1, respectively, i.e. at the fall of the monostable 104, whereupon a READY flip-flop 107 is set indicating receipt of a
5 new bit from the OID. The DATA flip-flop 108 is set or cleared depending on the line state at this time which is the same as the data bit value. When the sub-channel is accessed the contents of the flip-flops 107, 108 are applied to the internal buses 109 by gates 110. The DATA and READY flip-flops are cleared at T3 via gate 111
10 when the sub-channel is selected, i.e. immediately after transfer of their contents to the common DATA/READY circuits 112 of the parent channel board.

At time T2, the READY and DATA flip-flops 107, 108 of the selected sub-channel are clocked into the common DATA and READY flip-flops 113, 114 of the parent channel and these are applied via gates 115 to the
15 backplane line returning to the microsequencer.

The microsequencer can activate the 'line reverse' backplane line at 117 during a sub-channel cycle in order to activate the OID's red lamp and audio signal. The backplane BUS signal (LINE REVERSE/-EA) is
20 received on the channel board and routed to input 118 of each sub-channel circuit to trigger monostable 119 in the selected sub-channel circuit. This monostable stretches the pulse out to approximately 1/16 second and activates the bilateral switch 99 to reverse the line AB polarity. The other input of the monostable 119 is driven by the
25 sub-channel select line 120 so that only the correct sub-channel responds.

The Z80 board which controls the operation of the network multiplexer is shown in Figures 8A to 8J. At initialisation it downloads the micro-code into the microsequencer and causes it to perform a total system reset. Thereafter, the Z80 board receives message

5 blocks from the microsequencer, checks them and sends back an appropriate acknowledgement code. Good blocks are stored in its 256K byte memory for transmission to the host computer via the serial link.

The Z80 board is highly modular in design and layout. The board

10 contains the following functional blocks:

1. Central Processor Unit (CPU) 121
2. Read-only memory (ROM) 122
3. Random Access Memory (RAM) 123
4. Clock 125
- 15 5. Wait State/Reset Circuit 126,127
6. I/O Decoder 128
7. Memory mapping circuit 219
8. Counter Timer Chip (CTC) 130
9. Serial Interface (SIO) 131 to host computer
- 20 10. Parallel Interface (PIO) to Microsequencer 132
1. CPU

This is a standard 4MHz Z80 processor chip 121. No DMA operation is used so the address lines are latched and buffered in the outward direction only. The data lines are connected directly to the common

25 bus. The control lines are buffered outward.

2. ROM

The ROM array 122 consists of eight sockets for 2716-type EPROMS 124. After reset this array is mapped into the first 16K byte quadrant of the Z80 address range. CPU execution starts at location 5 zero. The board is designed on the assumption that the ROM program will copy all the operational code into the first 16K of RAM and will then transfer to it. The ROM loader does this by simultaneously switching the ROM off-line and the first 16K of RAM on-line using the parallel port controlling the memory map circuit. Thereafter the 10 ROM is not accessible by the CPU and performs no further function. The ROM data output is buffered to reduce capacitative loading.

3. RAM

This array is a standard arrangement of 4x8 64K dynamic RAM chips 123. The address bus to this array is eighteen bits wide and consists 15 of three (high-order) bits from the mapping circuit plus the low-order fifteen bits of the Z80 address bus.

4. Clock

This circuit is a standard 4MHz clock 125.

5. Wait State/Reset Circuit

20 These are standard Mostek circuits 126, 127. The Wait State function 126 is to insert one wait state in all memory accesses while the ROM is enabled. This only occurs during initialisation time and is due to the slow access time of the ROM chips.

The Reset circuit 127 is activated by power-on or external button. 25 For this board there is no need to preserve RAM contents on reset so a very simple circuit suffices.

6. I/O Decoder 128

Decodes the four port select codes (1-4) for the CTC, SIO, Microsequencer PIO, Mapping PIO from the address lines. This decoding is not exhaustive since there is no need for any more I/O chips than
5 those mentioned above.

7. Memory Mapping Circuit 129

The low-order four bits of the A port 136 of the Mapping PIO control this function. After reset these bits are all high. In this state the Z80 sees the ROM array in the low-order quadrant of its
10 address space and the RAM is disabled for any access to this or the next quadrant. It is intended that the ROM code will immediately set bits 3-1 to zero (leaving bit 0 high) and in this state the low-order 32K field of the RAM appears in the high-order half of the Z80 address space. Now the ROM loader can copy all the code to the low-order 32K
15 of the RAM where it will remain throughout normal running.

When the ROM loader is finished it will write zero to bit 0 of the port and instantly remove the ROM memory (and the wait states) and map the RAM field into the low-order half of the Z80 address space. The Z80 simply continues executing instructions but they are now
20 coming from the RAM. By storing the 3-bit address of one of the eight 32K RAM fields into bits 3-1 of the port the Z80 can access this field in the upper half of its address space.

8. CTC

Standard Z80 CTC chip 130. Channels 2 to 3 cascaded to form a
25 1 second clock. Channel 0 provides the SIO bit rate clock at 16 times 9600 baud.

9. SIO

A power circuit 133 using a charge pump produces plus/minus twelve volts for an RS232 interface. The SIO chip 131 provides two independent RS232 full duplex serial channels at 9600 baud.

5 10. PIO to Microsequencer

Standard buffered PIO 132. Port A 134 bidirectional, Port B 135 control output.

The ROM loader program is given in Appendix II.

The main Z80 program (Appendix III) consists, in essence, of a
10 simple endless background loop, as shown in the flow sheets of
Appendix IV, which interacts with five foreground interrupt routines.

After reset the program jumps to the label START and performs various initialisation functions as follows:

1. Set Z80 interrupt mode (mode 2)
- 15 2. Set I-register to point to the page containing the interrupt
vectors.
3. Set the SP-register to point to the top of the RAM area reserved
for the stack.
4. Initialise the values of the variables (zero except for the 'no.
20 of slots left' and 'serial number' fields).
5. Zero the parity/EOC work area.
6. Zero the entire sub-channel status area and transaction storage
area.
7. Set the IX-register to point to the parity work area (this
25 register stays constant).

8. Set the CTC vector to point to the one-second interrupt routine. Prepare the CTC channels 2 and 3 (in cascade) to interrupt at 1 second intervals.
9. Set the PIO interrupt vectors to point to the routines for input and output. Prepare the ports for A-bidirectional, B-control out (interrupts masked).
10. Set the SIO interrupt vector to point to the vector block labelled SIOVEC. Initialise the channel A control registers.
11. Copy the microcode from location 5000H (put there by the ROM loader) to the Writeable Control Store in the Microsequencer.
12. E RESET bit set.
13. Enable the microsequencer clock.
14. Wait 1/4 second or so for the microsequencer to reset itself.
15. Clear the reset flag so the microsequencer enters its normal cycle.
16. Perform a dummy PIO read to set the BRDY line in the Z80-microsequencer interface.
17. Branch to the background loop.

With reference to the background loop (as summarised in Appendix IV) it can be seen that in the absence of a complete input message block from either the microsequencer or the HP1000 (host) the Z80 is idling. The only significant function is the diagnostic display which consists of reading the eight-bit switch array, appending this byte to 41H to address a byte in the variable storage area, and displaying the contents of this address in the LED array.

The Z80 input routine from the host operates as follows:

- * There is a message block (labels begin HTI) defined for the 16-word host-multiplexer messages.
- * This is prefixed by a flag byte (HTIFLG) and a count byte (HTIBCT).
- * HTIFLG can take on the values 0-free, 1-busy (foreground), 2-busy (background).
- * When the SIO receives the first character the interrupt vectors into the SIARCA foreground routine. This aborts if HTIFLG is 2 (error) and sets HTIFLG to 1 if it is zero. The received character is stored in the message block at the byte corresponding to HTIBCT and the counter is incremented.
- * If the counter is 32 the entire message block has been received and HTIFLG is set to 2.
- * At this stage the background routine will accept the input message block for processing instead of bypassing that section of the code.
- * At the end of background processing HTIFLG and HTIBCT are set to zero so that the process can repeat when the host sends the next block:

The Z80 input routine from the microsequencer works in exactly the same way with the following exceptions.

1. The message block, flag and counter labels begin MSI.
 2. The message block length is 9 bytes consisting of the sub-channel address followed by the eight bytes of that sub-channel's RAM memory slot.
 3. The interrupt routine label is PIAIN.
- The Z80 output routine to the host is the inverse of the host input routine described above.

- * The labels begin with HTO.
- * The flag settings 1 and 2 have their meanings. Interchanged (actually 1 is not used).
- * The background routine initiates the operation, sets the byte counter to 1 and the flag to 2 and outputs the first character to the SIO chip.
- * When the SIO has sent this character it interrupts to location SIATBE. This foreground routine sends the next character and increments the counter.
- 10 * If SIATBE is entered with the counter equal to 32 the 'transmit buffer empty' condition is flushed, the counter and flag are set to zero and the operation is complete.

The Z80 output routine to the microsequencer is similar to the host output except:

- 15 1. The labels begin MSO
- 2. Since only one byte (the acknowledge code) is sent, the foreground routine simply flushes the resulting interrupt and clears the flag.
- 3. For the same reason the byte counter is superfluous.

As already discussed, the system has an HP1000 mini-computer at the center of a network of units with which it communicates via asynchronous serial links. These units will commonly have RS232 interfaces. RS232 interfaces are not rated for operation at distances greater than fifteen metres although, under favourable circumstances, they will sometimes function adequately up to three or four times that distance. However, in the factory environment for which the system is

25

intended, and particularly in view of the intended operation data rate (9600 baud), these interfaces are considered inadequate.

Certain more modern interfaces, in particular RS422 and its derivatives, operate using a balanced differential technique. Provided
5 the circuit is made using a single twisted pair telephone line, RS423 works well and at high speed. In spite of the enormous improvement which RS423 represents over RS232 it is still limited for factory use because there is a finite limit on the maximum tolerable common-mode noise on the line. For this reason, a fully isolated communication
10 technique has been adopted which uses optical isolators on the data lines and a transformer in the remote-end self-powering circuit. With this technique there is no DC connection whatsoever between the mini-computer ground and the remote terminal ground.

Figure 9 shows the electrical circuitry for a single channel.

15 Data circuit - local to remote:

The local (HP 1000) transmitter signal at 140 is received by a 26LS33 balanced differential receiver 141 and the resulting TTL signal drives a 26LS31 driver 142 which drives pair 1 in the cable. At the remote end the line pair is terminated by resistors 143 and a reverse-
20 clamped opto-isolator 144. The photo-transistor 145 activates a JFET high slew-rate operational amplifier 146 which produces an RS232-compatible signal at 147 for the terminal.

Data circuit - remote to local

The terminal RS232 signal at 148 is buffered by an LF352 (JFET op-
25 amp) circuit 149 which is differential and therefore provides better

noise immunity than normal. Thereafter, the circuit is the same as that used by the OMD readers and consists of an opto-isolator 150 driven by a transistor 151 and with its photo-transistor 152 connected in a Darlington pair with a further transistor 153 that shorts line
5 pair 2, drawing current symmetrically through two 120 ohm terminating resistors 154. The differential signal is decoded by a JFET op-amp circuit 155 which drives the RS232 receive data line 156. Since it is intended that there should be RS423 compatibility at this point the signal is clamped at 157 to approximately +/- 6 volts.

10 Power circuit.

Power is provided over the third pair of the 3-pair telephone cable to the remote interface box. This line pair is driven by a 12v DC source 158 grounded at the local end. The positive line is protected by a fuse 159. The supply is decoupled at the remote end by a
15 reservoir capacitor 160 and supplies the primary side 165 of a transformer 161. A CMOS oscillator 162 is set to run at approximately 50kHz and this signal switches the primary current in the transformer via a transistor 163. The centre-tapped fly-back voltage is clamped by a 20v Zener diode 164. The centre-tapped secondary coils 166 drive
20 two rectifier/stabiliser circuits 167 which produce the local + and - 12v supply referred to the terminal ground. The total current available is of the order of 20mA which is more than required by the local circuits.

The isolating adapter circuitry described is one of the factors
25 that makes the system particularly suitable for a works environment.

But there are numerous other features that contribute to this. The Operator Input Devices located at each work station are simple and inexpensive yet extremely robust, and the cards or tickets that they read are particularly cheap and easy to print. Yet the cards will
5 withstand considerable abuse - a card that has been screwed up or torn can still normally be reflatened and successfully read. Each OID, being parasitically supplied with power at a completely safe 24 volt level via its data transmission and control link, can be situated anywhere in the works. The MUXC receives data from the
10 OIDs that gives a complete and up-to-date picture of work in hand in the factory, showing the progress of particular orders, detecting break downs and bottle necks, recording employee attendances and work rates, and generally providing all the information necessary to plan the meeting of delivery targets, use the available personnel
15 and facilities in the most efficient manner, oversee the stock position, carry out payroll computations, and anticipate problems and take preventive action.

The microcomputers of the MUXC are provided with electric battery power supply back-up to prevent failure in the event of a
20 mains power interruption.

Various data formats used in the system are shown in Appendix V.

1. An operator input device (OID) for use in a system of production or work control, comprising a card reader for scanning a card or ticket bearing encoded data when said card is placed in the card reader and generating electrical signals representative of said encoded data, a cable for supplying low-voltage external electrical power to the OID over a pair of electrical lines, pulse train-generating-circuitry responsive to the card reader output signals to derive a stream of pulses of at least two different durations representing the encoded data, said pulse train-generating circuitry taking its electrical supply from said pair of lines, and short-circuiting means powered from said pair of lines and responsive to said stream of pulses to substantially short together said lines for a succession of time periods corresponding to the time durations of said pulses, whereby the data from the card or ticket is transmitted by the OID on the same cable pair as supplies the OID with its electrical power.
2. An OID according to claim 1, wherein said short-circuiting means is driven by an optical isolator having a radiation emitter to which said stream of pulses is applied, and a receiver responsive to the radiation from said emitter and electrically isolated therefrom, such as by diodes.
3. An OID according to claim 2, wherein said emitter is a light-emitting diode fed by a switching transistor to which the pulse stream is applied, said receiver is a photo-transistor, and said short-circuiting means is a switching transistor connected as a

Darlington pair with said photo-transistor.

4. An OID according to claim 1 or claim 2 or claim 3, wherein each card or ticket to be read bears black and white bar code, and the card reader comprises scanning means to illuminate the bar code tracks and sense the reflections therefrom.
5
5. An OID according to claim 4, wherein each card or ticket bears two parallel bar code tracks, the first being a clock track of regularly spaced thin bars, and the second a data track having either a thick bar or a space opposite each thin bar bit of the clock track
10 to indicate 'ones' and 'zeroes', and the scanning means comprises a first emitter/receiver combination scanning the clock track and a second emitter/receiver combination scanning the data track.
6. An OID according to claim 5, wherein each emitter/receiver combination comprises an infra red emitting diode and a photo-
15 transistor.
7. An OID according to claim 5 or claim 6, comprising two monostable circuits having different time periods to generate pulses of different widths, and logic circuitry responsive to the signals from the receivers of the scanning emitter/receivers to direct each clock
20 bit to the triggering input of one or other of the monostable circuits according to whether the data track is simultaneously showing a bar or a space.
8. An OID according to claim 7, wherein the outputs of the two monostable circuits are gated together to provide the stream of pulses
25 that is applied to the transistor feeding the light-emitting diode of

the optical isolator.

9. An OID according to any one of the preceding claims, further comprising audio and/or visual response means which is energized by the external power supply cable when the polarity of the voltage on the cable line pair is reversed.
10. An OID according to claims 3, 5 and 9, wherein the OID circuits associated with the scanning emitter/receivers, generating the pulse stream and feeding the emitter diode of the optical isolator are powered from lines maintained at a predetermined voltage by a storage capacitor and voltage regulator, the storage capacitor on the one hand and the audio and/or visual response means on the other hand being supplied from the common line pair of the external supply cable via reversely poled isolating diodes.
11. A production or work control system for a works environment, comprising a multiplicity of operator input devices (OIDs) situated at the work stations of human operatives and each having a card reader; and a multiplexor/concentrator consisting of the combination of a microcomputer and a microprocessor, the microprocessor comprising a microsequencer repeatedly scanning the OIDs in a continuous operation to acquire data therefrom which is passed to the microcomputer, the microcomputer carrying out validity checking on the data input from the OIDs by the microsequencer, storing good data in short-term store and returning to the microsequencer signals indicative of the validity or otherwise of each data input consequent upon a card reading at an OID, the microsequencer returning to the

individual OIDs the signals indicative of the validity or otherwise of their data inputs, and the microcomputer having input and output ports for communication with a host computer, such as a minicomputer.

12. A system according to claim 11 wherein the microprocessor/
5 microsequencer is a bipolar bit-slicing microprocessor of the single-level pipelined type.

13. A system according to claim 11 or claim 12, wherein the microcomputer is a Z80 computer board.

14. A system according to claim 11 or claim 12 or claim 13, wherein
10 the microsequencer communicates with the multiplicity of OIDs via a group of channels each of which services a respective group of sub-channels, there being an individual sub-channel for each OID.

15. A system according to any one of claims 11 to 14, wherein the card reader of each OID reads bar code tracks printed on cards or
15 tickets passed through the card reader by the operative.

16. A system according to claim 15, wherein there are three types of card or ticket:

- i) operator cards or badges identifying individual operatives
- ii) operation cards indicating particular work operations
20 being performed
- iii) job lot cards or tickets identifying batches of work.

17. A system according to any one of claims 11 to 16, wherein the communication between an OID and a respective sub-channel of the microsequencer is via a single twisted pair cable over which the OID
25 also receives its power supply at a safe voltage parasitically from

the microsequencer.

18. A system according to any one of claims 11 to 17, wherein the microsequencer supplies power to each individual OID by maintaining a voltage on a respective pair of lines, and the OID communicates
5 data to the microsequencer by substantially shorting out said lines temporarily for pulse periods having two different time durations.

19. A system according to claim 18, wherein after receiving the data on a card read by an OID the microsequencer transmits the signals from the microcomputer indicative of the validity of the data to
10 the respective OID by pulses generated by momentarily reversing the polarity of the power lines.

20. A system according to any one of claims 11 to 19, wherein the validity checking of data from an individual OID includes a check as to whether the operative at the work station of the OID has
15 inserted a plurality of different cards in the card reader in the correct order.

21. A system according to any one of claims 11 to 20, wherein each OID is an operator input device according to any one of claims 1 to 10.

20 22. A serial link for communication over distances between a host computer and a microcomputer or a terminal, comprising a two-pair cable each pair providing a one-way communication channel and including an optical isolator.

23. A link according to claim 22, wherein the host to microcomputer/
25 terminal channel comprises a chain including, in succession, a balanced

differential receiver-driver-cable pair-clamped optical isolator-
operational amplifier; and the microcomputer/terminal to host channel
comprises a chain including, in succession, an operational amplifier-
optical isolator-line-shortening transistor-cable pair-operational
5 amplifier decoder-clamped output circuit.

24. A link according to claim 22 or claim 23, including a third
cable pair for supplying power from the host to the microcomputer/
terminal, the power supply chain including, in succession, a host
power source-cable pair-oscillator-transformer- rectifying and
10 stabilising circuit.

25. A system according to any one of claims 11 to 21, including a
microcomputer to host minicomputer link according to any one of claims
22 to 24, the microcomputer and microprocessor also having electric
battery supply back-up to overcome mains power interruptions.

APPENDIX I

MOSTEK MACRO-80 ASSEMBLER V2.2

LOC OBJ. CODE STMT-NR SOURCE-STMT PASS2 Z25J1 Z25J1 Z25J1 ABS

```

1          TITLE MICROCODE FOR PCI SEQUENCER
;:::::::          ::::::::::
3          PSECT ABS
; LIST 0
=0000      5 NONE   EQU 0
=0004      6 RO     EQU 04H
=0008      7 PI     EQU 0BH
=000C      8 LA     EQU 0CH
=0010      9 HA     EQU 10H
=0014     10 LAE    EQU 14H
=0018     11 E      EQU 18H
=0000     12 D      EQU 0
=0001     13 POD    EQU 1
=0002     14 RI     EQU 2
=0003     15 T      EQU 3
=0000     16 X      EQU 0      ;::::::: FOR UNUSED FIELDS ::::::::::
=0000     17 NOP    EQU 0
=0040     18 RAMF   EQU 40H
=0080     19 RAMD   EQU 80H
=00C0     20 RAMU   EQU 0COH
=0020     21 AND    EQU 20H
=001E     22 OR     EQU 18H
=0030     23 XOR    EQU 30H
=0000     24 ADD    EQU 0
=0008     25 SUBR   EQU 8
=0007     26 DZ     EQU 7
=0005     27 DA     EQU 5
=0004     28 ZA     EQU 4
=0001     29 AB     EQU 1
=0020     30 R      EQU 20H
=0010     31 S      EQU 10H
=0002     32 RDYI   EQU 2
=0001     33 RDYA   EQU 1

```

```

=0080    34 RESET EQU 80H
=0040    35 Z      EQU 40H
=0020    36 HZ     EQU 20H
=0010    37 LZ     EQU 10H
=0008    38 F3H    EQU 8
=0004    39 F3L    EQU 4
=0002    40 ER     EQU 2
=0001    41 TT     EQU 1

; ::::::::::: START OF MACRO DEFINITIONS
43 DD     MACRO #DOUT, #DIN, #ID, #IFN, #IS, #B, #A, #D
1 44      DEFB #DOUT+ #DIN, #ID+ #IFN+ #IS, #B #16+ #A, #D
2 45      MEND

; :::::::::::
47 BRDY   MACRO #R, #S, #RDM, #ADDR
1 48      DEFB 1CH, #R+ #S+ #RDM, 0, #ADDR/4 ; >>>> #ADDR
2 49      MEND

; :::::::::::
51 BM     MACRO #R, #S, #M, #ADDR
1 52      DEFB 1CH, #R+ #S, #M, #ADDR/4 ; >>>> #ADDR
2 53      MEND

; :::::::::::
55 BM7    MACRO #R, #S, #M, #ADDR
1 56      DEFB 0FCH, #R+ #S, #M, #ADDR/4 ; >>>> #ADDR
2 57      MEND

; :::::::::::
59 BPT    MACRO
1 60      DEFB 0,0,0,0 ; PATCHABLE B/PT
2 61      MEND

; ::::::::::: END OF MACRO DEFINITIONS
;
; LIST 1
65        CLIST 0
;
; FORMAT FOR MACRO EXPANSIONS:
; NON-BRANCH
; DD DOUT,DIN, IDEST,IFUNC,ISOURCE,BREG,AREG, DATA

```

```

; BRANCH WITH I/O READY TEST:
; BRDY REVERSE SENCE,8-WAY BRANCH,FLAG NAME, ADDRESS
;
; (NOTE ADDRESS PUT IN BY HAND)
; BRANCH WITH OTHER TESTS:
; BM REVERSE SENSE,8-WAY BRANCH,FLAG NAME, ADDRESS
;
; DATA RAM IS ORGANISED AS 128 SLOTS OF 8 BYTES
; THERE IS ONE SLOT FOR EACH SUB-CHANNEL.
; THE BYTES IN EACH SLOT ARE AS FOLLOWS:
; 0: STATE/TIME (FORMAT SSSOTTTT)
; 1: CURRENT BIT/CELL (FORMAT OBBBOCCC)
; COUNTS SHIFTING IN OF DATA,
; STARTS AT 02H AND COUNTS UP.
; 2: FIRST DATA BYTE. INITIALLY USED TO
; ACCUMULATE THE SYN CHARACTER WHICH
; IS THEN OVERLAYED BY THE FIRST DATA BYTE.
; 3-7: REMAINING DATA AND CHECK BYTES.
;
;
; REGISTER USAGE:
; R0: COUNTER FOR SUB-CHANNEL (KKKKKKKO)
; R1: STATE/TIME (SSSOTTTT)
; R2: BIT/CELL (OBBBOCCC)
; R3: DATA BYTE
; R4: COUNTER FOR RESET RAM CLEARING ROUTINE
; R5: LA-REGISTER
; R6: WORK REGISTER
;
; R12: ACKNOWLEDGE CODE (0=OK,1=PHYSICAL ERROR,
; 2=LOGICAL ERROR)
; R13: CELL NO FOR Z80 TRANSFER
; R14: SUB-CHANNEL (KKKKKKKO) FOR Z80 TRANSFER
; R15: XOOOYOOO WHERE X=1 IF Z80 XFER IS BUSY AND
; Y=0 BEFORE XFER OF SUB-CHANNEL
; NUMBER TO THE Z80.
;

```

```

;::::::::::::::::::::::::::::::::::::::::::::::::::
;::::::::::::::::::::::::::::::::::::::::::::::::::::
;
;HARDWARE FORCES START AT THIS POINT AFTER
;Z80 HAS DOWN-LOADED THE MICROCODE AND THEN
;ACTIVATED THE 'SEQUENCER RUN' AND
;'CLOCK ENABLE' LINES ON PORT B.
;
;ALL STATE PROCESSORS RETURN HERE TO SELECT THE NEXT
; SUBCHANNEL
;

```

116 LIST 1

```

;::::::::::::::::::::::::::::::::::::::::::::::::::
0000 118 START BM7 R,X,X,STROOL;NORMALLY SKIP OVER LOG-
      OUT STB 7
0000 FC200014 1 119 DEFB OFCH,R+X,STROOL/4; >>>> STROOL
0004 119 121 DD NONE,D,NOP,XOR,DA,X,0,0 ;TEST FOR
      GIVEN S/C ENTER TWICE DESIRED S/C
0004 00350000 1 122 DEFB NONE+D,NOP+XOR+DA,X 16+0,0
0008 120 124 BM R,X,Z,STROOL ;SKIP LOG-OUT IF NOT
      DESIRED S/C
0008 1C204014 1 125 DEFB 1CH,R+X,Z,STROOL/4 ; >>>> STROOL
000C 121 127 DD LA,D,RAMF,OR,DZ,5,X,0 ;LA,R5<0
000C 0C5F5000 1 128 DEFB LA+D,RAMF+OR+DZ,5 16+X,0
0010 122 130 DD NONE,RI,NOP,OR,DZ,X,X,X
0010 021F0000 1 131 DEFB NONE+RI,NOP+OR+DZ,X 16+X,X
0014 123 133 DD LA,D,RAMF,OR,DZ,5,X,1
0014 0C5F5001 1 134 DEFB LA+D,RAMF+OR+DZ,5 16+X,1
0018 124 136 DD NONE,RI,NOP,OR,DZ,X,X,X
0018 021F0000 1 137 DEFB NONE+RI,NOP+OR+DZ,X 16+X,X
001C 125 139 DD LA,D,RAMF,OR,DZ,5,X,2
001C 0C5F5002 1 140 DEFB LA+D,RAMF+OR+DZ,5 16+X,2
0020 126 142 DD NONE+20H,RI,NOP,OR,DZ,X,X,X ; STB 1
0020 221F0000 1 143 DEFB NONE+20H+RI,NOP+OR+DZ,X 16+X,X
0024 127 145 DD LA,D,RAMF,OR,DZ,5,X,3
0024 0C5F5003 1 146 DEFB LA+D,RAMF+OR+DZ,5 16+X,3

```

```

0028          128 148      DD NONE+40H,RI,NOP,OR,DZ,X,X,X ; 1#STB
                                2##
0028 421F0000      1 149      DEFB NONE+40H+RI,NOP+OR+DZ,X# 16+X,X
002C          129 151      DD LA,D,RAMF,OR,DZ,5,X,4
002C 0C5F5004      1 152      DEFB LA+D,RAMF+OR+DZ,5# 16+X,4
0030          130 154      DD NONE+60H,RI,NOP,OR,DZ,X,X,X ; 1#STB
                                3##
0030 621F0000      1 155      DEFB NONE+60H+RI,NOP+OR+DZ,X# 16+X,X
0034          131 157      DD LA,D,RAMF,OR,DZ,5,X,5
0034 0C5F5005      1 158      DEFB LA+D,RAMF+OR+DZ,5# 16+X,5
0038          132 160      DD NONE+80H,RI,NOP,OR,DZ,X,X,X ; 1#STB
                                4##
0038 821F0000      1 161      DEFB NONE+80H+RI,NOP+OR+DZ,X# 16+X,X
003C          133 163      DD LA,D,RAMF,OR,DZ,5,X,6
003C 0C5F5006      1 164      DEFB LA+D,RAMF+OR+DZ,5# 16+X,6
0040          134 166      DD NONE*0A0H,RI,NOP,OR,DZ,X,X,X ; 1#STB
                                5##
0040 A21F0000      1 167      DEFB NONE+0A0H+RI,NOP+OR+DZ,X# 16+X,X
0044          135 169      DD LA,D,RAMF,OR,DZ,5,X,7
0044 0C5F5007      1 170      DEFB LA+D,RAMF+OR+DZ,5# 16+X,7
0048          136 172      DD NONE+0C0H,RI,NOP,OR,DZ,X,X,X ; 1#STB
                                6##
0048 C21F0000      1 173      DEFB NONE+0C0H+RI,NOP+OR+DZ,X# 16+X,X
004C          137 175      BM R,X,X,DIAGCN
004C 1C20008E      1 176      DEFB 1CH,R+X,X,DIAGCN/4 ; >>>> DIAGCN
                                ;
0050          139 179 STROO1 BM X,X,RESET,RSTOOO ; TO RESET IF FLAG ON
0050 1C008069      1 180      DEFB 1CH,X+X,RESET,RSTOOO/4 ; >>>> RSTOOO
0054          140 182      DD LAE,D,RAMF,OR,DZ,5,X,40H ;EA,ET,LA,
                                R5<0 , EC<1
0054 145F5040      1 183      DEFB LAE+D,RAMF+OR+DZ,5# 16+X,40H
0058          141 185      DD HA,D,RAMF,ADD,DA,O,O,2 ;HA,RO<RO+2
0058 10450002      1 186      DEFB HA+D,RAMF+ADD+DA,O# 16+O,2
005C          142 188      BM R,X,Z,STROOO ;SKIP 2 IF S/C# O
005C 1C20401B      1 189      DEFB 1CH,R+X,Z,STROOO/4 ; >>>> STROOO
0060          143 191      DD E,D,NOP,OR,DZ,X,X,60H ;ET<1 PULSE ET
                                WHILE

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0060 181F0060      1 192      DEFB E+D,NOP+OR+DZ,X# 16+X,60H
0064              144 194      DD E,D,NOP,OR,DZ,X,X,40H ;ET<O -EC STAYS 1
0064 181F0040      1 195      DEFB E+D,NOP+OR+DZ,X# 16+X,40H
0068              145 197      DD NONE,X,NOP,X,X,X,X,X ;NOP TO EXTEND EC
0068 00000000      1 198      DEFB NONE+X,NOP+X+X,X# 16+X,X
006C              146 200 STROOO DD LAE,D,RAMF,OR,DZ,5,X,O ;EA,EC,ET,LA,
                                R5<O
006C 145F5000      1 201      DEFB LAE+D,RAMF+OR+DZ,5# 16+X,O
0070              147 203      DD NONE,RI,RAMF,OR,DZ,1,X,X ;R1<STATE/TIME
                                THIS S/C
0070 025F1000      1 204      DEFB NONE+RI,RAMF+OR+DZ,1# 16+X,X
0074              148 206      BM R,S,HZ,O ;8 WAY BRANCH TO SSSOOOO
                                IF SSS# 0
0074 1C302000      1 207      DEFB 1CH,R+S,HZ,O/4 ; >>>> 0
0078              149 209      BM R,X,ER,START ; TO START IF ER=0 IE NO
                                REQUEST
0078 1C200200      1 210      DEFB 1CH,R+X,ER,START/4 ; >>>> START
007C              150 212      DD RO,D,RAMF,OR,DZ,1,X,2FH ;RAMO,R1<2VH;
                                SET STATE 1 AND TIME-OUT VALUE
007C 045F102F      1 213      DEFB RO+D,RAMF+OR+DZ,1# 16+X,2FH
                                ;;; BM R,X,X,ST1000 ;BRANCH TO THE STATE 1 ENTRY
                                PT ;,DROP THROUGH
                                ;EITHER THIS BRANCH OR THE 8 WAY BRANCH 3 STMTS
                                ; BACK
                                ;CAUSES AN ADVANCE TO ADDRESS SSSOOOO (S=STATE)
                                ;WITH EA,EC,ET,LA,R5=0: RO,HA=KKKKKKKO WHERE
                                ;K IS THE SUB-CHANNEL; R1,RAMO(K)=SSSOVVVV WHERE
                                ;SSS IS THE STATE AND VVVV IS THE INITIAL VALUE
                                ;OF THE TIME-OUT.
                                ;::::::::::::::::::::::::::::::::::::::::::
0080              159 223      ORG 80H ;WORD ADDRESS 20H, ENTRY FOR
                                STATE 1
                                ;STATE 1: READING BUT NOT YET READ SYN CHARACTER
0080              161 225      ST1000 BPT
0080 00000000      1 226      BM R,X,ER,ST1001 ;TO ST1001 IF ER=0 IE
                                NO REQUEST

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0084      162  228      DEFB 1CH,R+X,ER,ST1001/4 ; >>>> ST1001
0084 1C200228      1  229      DD RO,D,RAMF,OR,DZ,1,X,2FH
0088      163  231      DD LA,D,RAMF,OR,DZ,5,X,2 ;R5,LA<2
0088 0C5F5002      1  232      DEFB LA+D,RAMF+OR+DZ,5#16+X,2
008C      164  234      DD NONE,RI,RAMD,OR,DZ,3,X,X ;R3<ED, HI 7
                                BITS OF RAM2(K)
008C 029F3000      1  235      DEFB NONE+RI,RAMD+OR+DZ,3#16+X,X
                                ;SHIFTS CONTENTS OF RAM2(K) DOWN ONE PLACE WITH
                                ;THE DATA BIT ED ENTERING IN BIT 7
0090      167  239      DD RO,X,NOP,OR,ZA,X,3,X ;RAM2(K)<R3
                                UPDATE RAM
0090 041C0300      1  240      DEFB RO+X,NOP+OR+ZA,X#16+3,X
0094      168  242      DD NONE,D,NOP,SUBR,DA,X,3,15H ;SUBTRACT
                                SYN CHAR
0094 000D0315      1  243      DEFB NONE+D,NOP+SUBR+DA,X#16+3,15H
0098      169  245      BM R,X,Z,ST1001 ;SKIP 1 IF #SYN
0098 1C204028      1  246      DEFB 1CH,R+X,Z,ST1001/4 ; >>>> ST1001
009C      170  248      DD NONE,D,RAMF,ADD,DA,1,1,20H ;R1<STATE
                                2,TIME SAME
009C 00451120      1  249      DEFB NONE+D,RAMF+ADD+DA,1#16+1,20H
00A0      171  251 ST1001 DD LA,D,RAMF,OR,DZ,5,X,0 ;R5,LA<0
00A0 0C5F5000      1  252      DEFB LA+D,RAMF+OR+DZ,5#16+X,0
00A4      172  254      DD RO,T,RAMF,SUBR,ZA,1,1,X ;DECR R1,RAMO
                                IF T=1
00A4 074C1100      1  255      DEFB RO+T,RAMF+SUBR+ZA,1#16+1,X
                                ;REDUCE TIME OUT VALUE BY ONE IF THIS IS A TIMER
                                ;CYCLE
00A8      174  258      BM R,X,LZ,START ;TO START IF NOT TIMED
                                OUT
00A8 1C201000      1  259      DEFB 1CH,R+X,LZ,START/4 ; >>>> START
00AC      175  261 ST1002 DD RO,D,RAMF,OR,DZ,1,X,60H ;STATE 3
00AC 045F1060      1  262      DEFB RO+D,RAMF+OR+DZ,1#16+X,60H
00B0      176  264      BM R,X,X,START ;TO START
00B0 1C200000      1  265      DEFB 1CH,R+X,X,START/4 ; >>>> START
                                ;
                                ;CONTINUATION OF STATE 5 CODE FOR ACK 2
                                ;(LOGICAL ERROR)

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```

OOB4      179 269 ST5003 DD LA,D,RAMF,OR,DZ,5,X,7 ;LA,R5<7
OOB4 OC5F5007      1 270 DEFB LA+D,RAMF+OR+DZ,5*16+X,7
OOB8      180 272 DD RO,X,NOP,OR,DZ,X,X,OC0H
OOB8 041F00C0      1 273 DEFB RO+X,NOP+OR+DZ,X*16+X,OC0H
OOBC      181 275 DD LA,D,RAMF,OR,DZ,5,X,6
OOBC OC5F5006      1 276 DEFB LA+D,RAMF+OR+DZ,5*16+X,6
OOCO      182 278 DD RO,X,NOP,OR,DZ,X,X,OC9H
OOCO 041F00C9      1 279 DEFB RO+X,NOP+OR+DZ,X*16+X,OC9H
OOC4      183 281 DD LA,D,RAMF,OR,DZ,5,X,5
OOC4 OC5F5005      1 282 DEFB LA+D,RAMF+OR+DZ,5*16+X,5
OOC8      184 284 DD RO,X,NOP,OR,DZ,X,X,OE1H
OOC8 041F00E1      1 285 DEFB RO+X,NOP+OR+DZ,X*16+X,OE1H
OCCC      185 287 DD LA,D,RAMF,OR,DZ,5,X,4
OCCC OC5F5004      1 288 DEFB LA+D,RAMF+OR+DZ,5*16+X,4
OODO      186 290 DD RO,X,NOP,OR,DZ,X,X,OE4H ;ABOVE CODE
FOR DAH-DI-DAH TONE
OODO 041F00E4      1 291 DEFB RO+X,NOP+OR+DZ,X*16+X,OE4H
OOD4      187 293 DD NONE,D,RAMF,OR,DZ,6,X,4 ;R6<4 START
CELL
OOD4 005F6004      1 294 DEFB NONE+D,RAMF+OR+DZ,6*16+X,4
OOD8      188 296 BM R,X,X,ST5002 ;TO EXIT ROUTINE
OOD8 1C2000A7      1 297 DEFB 1CH,R+X,X,ST5002/4 ; >>>> ST 5002
;
;:.....:
O100      191 301 ORG 100H ;WORD ADDRESS 40H,ENTRY FOR
STATE 2
;STATE 2:READING AFTER DETECTION OF SYN
O100      193 303 ST2000 BPT
O100 00000000      1 304 BM R,X,ER,ST1001 ;TO ST1001 IF NO REQUEST
O104      194 306 DEFB 1CH,R+X,ER,ST1001/4 ; >>>> ST1001
O104 1C200228      1 307 DD RO,D,RAMF,OR,DZ,1,X,4FH
O108      195 309 DD LA,D,RAMF,OR,DZ,5,X,1 ;R5,LA<1 (BIT/
CELL BYTE)
O108 OC5F5001      1 310 DEFB LA+D,RAMF+OR+DZ,5*16+X,1
O10C      196 312 DD NONE,RI,RAMF,OR,DZ,2,X,X ;R2<BC
O10C 025F2000      1 313 DEFB NONE+RI,RAMF+OR+DZ,2*16+X,X

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0110	197	315	DD NONE,X,RAMF,OR,ZA,6,2,X ;R6<R2 WORK REG
0110 005C6200	1	316	DEFB NONE+X,RAMF+OR+ZA,6#16+2,X
0114	198	318	DD NONE,D,RAMF,ADD,DA,2,2,10H;R2<R2+10H NEXT BIT
0114 00452210	1	319	DEFB NONE+D,RAMF+ADD+DA,2#16+2,10H
0118	199	321	BM R,X,F3H,ST2001 ;SKIP IF R2 still <=7
0118 1C200848	1	322	DEFB 1CH,R+X,F3H,ST2001/4 ; >>>> ST2001
011C	200	324	DD NONE,D,RAMF,ADD,DA,2,2,81H ; ELSE TO BITO NEXT CELL
011C 00452281	1	325	DEFB NONE+D,RAMF+ADD+DA,2#16+2,81H
0120	201	327 ST2001	DD RO,X,NOP,OR,ZA,X,2,X ;RAM 1<R2 UPDATE RAM
0120 041C0200	1	328	DEFB RO+X,NOP+OR+ZA,X#16+2,X
0124	202	330	DD LA,X,NOP,OR,ZA,C,6,X ;LA<R6 IE LA IS CELL BEFORE UPDATE
0124 0C1C0600	1	331	DEFB LA+X,NOP+OR+ZA,X#16+6,X
0128	203	333	DD NONE,RI,RAMD,OR,DZ,3,X,X ;R3<ED,HI 7 BITS OF BYTE C
0128 029F3000	1	334	DEFB NONE+RI,RAMD+OR+DZ,3#16+X,X
012C	204	336	DD RO,X,NOP,OR,ZA,X,3,X ;RAMC<R3 UPDATE BYTE C
012C 041C0300	1	337	DEFB RO+X,NOP+OR+ZA,X#16+3,X
0130	205	339	DD LA,D,RAMF,OR,DZ,5,X,0 ;R5,LA<0
0130 0C5F5000	1	340	DEFB LA+D,RAMF+OR+DZ,5#16+X,0
0134	206	342	DD RO,T,RAMF,SUBR,ZA,1,1,X ;DECR R1,RAMO IF T=1 (TIMER CYCLE)
0134 074C1100	1	343	DEFB RO+T,RAMF+SUBR+ZA,1#16+1,X
0138	207	345	BM X,X,LZ,ST1002 ;TO ST1002 (SET STATE 3) IF TIMED OUT
0138 1C00102B	1	346	DEFB 1CH,X+X,LZ,ST1002/4 ; >>>> ST1002
013C	208	348	DD NONE,X,NOP,OR,ZA,X,2,X ;SET STATS FOR R2 (UPDATE BC BYTE)
013C 001C0200	1	349	DEFB NONE+X,NOP+OR+ZA,X#16+2,X
0140	209	351	BM R,X,F3L,START ;TO SATRT IF CELL STILL <=7

```

;
;THE RESET ROUTINE IS FITTED IN HERE SINCE THE
;STATE 3 PROCESSOR IS THE SHORTEST
;

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;RESET ROUTINE:

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;
OLA4      230 396 RSTOOO BPT
OLA4 00000000      1 397      DEFB O,O,O,O ;PATCHABLE B/PT
OLA8      231 399      DD E,X,RAMF,AND,ZA,O,X,X ;E,RO<O
OLA8 18640000      1 400      DEFB E+X,RAMF+AND+ZA,O#16+X,X
OLAC      232 402      DD HA,X,NOP,OR,ZA,X,O,X ;HA<RO IE O
OLAC 101C0000      1 403      DEFB HA+X,NOP+OR+ZA,X#16+O,X
OLBO      233 405 RSTOOL DD LA,X,NOP,AND,ZA,X,X,X ;LA<O
OLBO OC240000      1 406      DEFB LA+X,NOP+AND+ZA,X#16+X,X
OLB4      234 408      DD RO,D,NOP,OR,DZ,X,X,OFH ;RAMO<STATE O,
                                T/O=15
OLB4 041F000F      1 409      DEFB RO+D,NOP+OR+DZ,X#16+X,OFH
OLB8      235 411      DD LA,D,RAMF,OR,DZ,5,X,1 ;LA,R5<1
OLB8 OC5F5001      1 412      DEFB LA+D,RAMF+OR+DZ,5#16+X,1
OLBC      236 414      DD RO,D,NOP,OR,DZ,X,X,O2H :RAM1<2 SET
                                BIT/CELL BYTE
OLBC 041F0002      1 415      DEFB RO+D,NOP+OR+DZ,X#16+X,O2H
OLCO      237 417      DD NONE,D,RAMF,OR,DZ,4,X,6 ;R4<6 COUNTER
                                FOR REMAINING BYTES
OLCO 005F4006      1 418      DEFB NONE+D,RAMF+OR+DZ,4#16+X,6
OLC4      238 420      DD LA,D,RAMF,OR,DZ,5,X,2 ;LA,R5<2
OLC4 OC5F5002      1 421      DEFB LA+D,RAMF+OR+DZ,5#16+X,2
OLC8      239 423 RSTOOL DD RO,D,NOP,OR,DZ,X,X,O ;RAM(R4)<O CLEAR
                                DATA BYTE
OLC8 041F0000      1 424      DEFB RO+D,NOP+OR+DZ,X#16+X,O
OLCC      240 426      DD LA,D,RAMF,ADD,DA,5,5,1 ;LA,R5<R5+1
                                INC RAM ADDR
OLCC OC455501      1 427      DEFB LA+D,RAMF+ADD+DA,5#16+5,1
OLDO      241 429      DD NONE,D,RAMF,SUBR,DA,4,4,0 ;DECREMENT
                                COUNTER
OLDO 004D4400      1 430      DEFB NONE+D,RAMF+SUBR+DA,4#16+4,0
OLD4      242 432      BM R,X,Z,RSTOOL ;LOOP BACK IF COUNT NOT O
OLD4 1C204072      1 433      DEFB 1CH,R+X,Z,RSTOOL/4 ; >>>> RSTOOL
OLD8      243 435      DD HA,D,RAMF,ADD,DA,O,O,2 ;HA,RO<RO+2
                                NEXT S/CHAN

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01D8 10450002      1  436      DEFB HA+D,RAMF+ADD+DA,0#16+0,2
01DC                244 438      BM R,X,Z,RSTOOL ;OUTER LOOP BACK IF S/C
                                NOT 0
01DC 1C20406C      1  439      DEFB 1CH,R+X,Z,RSTOOL/4 ; >>>> RSTOOL
01EO                245 441      DD HA,D,RAMF,SUBR,DA,0,0,1 ;HA,RO BACK TO
                                254 SO
01EO 104D0001      1  442      DEFB HA+D,RAMF+SUBR+DA,0#16+0,1
                                ;
                                NEXT INCR WILL MAKE 0
01E4                247 445      DD NONE,D,RAMF,OR,DZ,15,X,0 ;R15<0 Z80
                                BUSY FLAG CLEAR
01E4 005FF000      1  446      DEFB NONE+D,RAMF+OR+DZ,15#16+X,0
01EB                248 448      BM R,X,X,RSTOOL3 ;TO CONTINUATION OF RESET
                                ROUTINE
01EB 1C2000EB      1  449      DEFB 1CH,R+X,X,RSTOOL3/4 ; >>>> RSTOOL3
                                ;
                                ;::::::::::::::::::::::::::::::::::::::::::
0200                251 453      ORG 200H ;WORD ADDRESS 80H, ENTRY FOR
                                STATE 4
                                ;STATE 4: Z80 TRANSFER
0200                253 455 ST4000 BPT
0200 00000000      1  456      DEFB 0,0,0,0 ;PATCHABLE B/PT
0204                254 458      BRDY R,X,RDYI,START ;TO START IF NOT
                                READY FOR INPUT
0204 1C220000      1  459      DEFB 1CH,R+X+RDYI,0,START/4 ; >>>> START
0208                255 461      DD NONE,X,NOP,OR,ZA,X,15,X ;STATS OF R15
0208 001C0F00      1  462      DEFB NONE+X,NOP+OR+ZA,X#16+15,X
020C                256 464      BM X,X,F3L,ST4001 ;BR TO ST4001 IF Y=1
                                IE S/C BYTE HAS BEEN SENT
020C 1C000487      1  465      DEFB, 1CH,X+X,F3L,ST4001/4 ; >>>> ST4001
0210                257 467      DD PI,X,NOP,OR,ZA,X,14,X ;SEND R14 to PIO
                                A INPUT TO Z80
0210 081C0E00      1  468      DEFB PI+X,NOP+OR+ZA,X#16+14,X
0214                258 470      DD NONE,D,RAMF,OR,DA,15,15,8 ;SET Y=1 TO
                                INDICATE S/C SENT
0214 005DFF08      1  471      DEFB NONE+D,RAMF+OR+DA,15#16+15,8
0218                259 473      BM R,X,X,START ;TO START

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0218 1C200000      1 474      DEFB 1CH,R+X,X,START/4 ; >>>> START
021C                260 476 ST4001 DD LA,X,RAMF,OR,ZA,5,13,X ;R5,LA<R13
                                CELL FOR XFER
021C OC5C5D00      1 477      DEFB LA+X,RAMF+OR+ZA,5#16+13,X
0220                261 479      DD PI,RI,NOP,OR,DZ,X,X,X ;SEND CONTENTS
                                OF CELL TO PIO A
0220 OA1F0000      1 480      DEFB PI+RI,NOP+OR+DZ,X#16+X,X
0224                262 482      DD NONE,D,RAMF,ADD,DA,13,13,1 ;INCR R13
                                TO NEXT CELL
0224 OO45DD01      1 483      DEFB NONE+D,RAMF+ADD+DA,13#16+13,1
0228                263 485      BM R,X,F3L,START ;TO START IF CELL
                                STILL <=7
0228 1C200400      1 486      DEFB 1CH,R+X,F3L,START/4 ; >>>> START
022C                264 488      DD LA,D,RAMF,OR,DZ,5,X,O ;R5,LA<O ADDRESS
                                S/T BYTE
022C OC5F5000      1 489      DEFB LA+D,RAMF+OR+DZ,5#16+X,O
0230                265 491      DD RO,D,RAMF,OR,DZ,1,X,OA0H ;R1,RAM0<AO
                                IE STATE 5
0230 O45F10A0      1 492      DEFB RO+D,RAMF+OR+DZ,1#16+X,OA0H
0234                266 494      BM R,X,X,START ;TO START
0234 1C200000      1 495      DEFB 1CH,R+X,X,START/4 ; >>>> START
                                ; REGISTER LOG-OUT PART OF DIAGNOSTICS
0238                268 498 DIAGCN BPT
0238 00000000      1 499      DEFB O,O,O,O ;PATCHABLE B/PT
023C                269 501      DD NONE,X,NOP,OR,ZA,X,O,X ;RO
023C 001C0000      1 502      DEFB NONE+X,NOP+OR+ZA,X#16+O,X
0240                270 504      DD NONE,X,NOP,OR,ZA,X,1,X ;R1
0240 001C0100      1 505      DEFB NONE+X,NOP+OR+ZA,X#16+1,X
0244                271 507      DD NONE,X,NOP,OR,ZA,X,2,X ;R2
0244 001C0200      1 508      DEFB NONE+X,NOP+OR+ZA,X#16+2,X
0248                272 510      DD NONE,X,NOP,OR,ZA,X,3,X ;R3
0248 001C0300      1 511      DEFB NONE+X,NOP+OR+ZA,X#16+3,X
024C                273 513      DD NONE,X,NOP,OR,ZA,X,4,X ;R4
024C 001C0400      1 514      DEFB NONE+X,NOP+OR+ZA,X#16+4,X
0250                274 516      DD NONE,X,NOP,OR,ZA,X,5,X ;R5
0250 001C0500      1 517      DEFB NONE+X,NOP+OR+ZA,X#16+5,X

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0254          276 520      DD NONE,X,NOP,OR,ZA,X,12,X ;R12
0254 001C0COO      1 521      DEFB NONE+X,NOP+OR+ZA,X#16+12,X
0258          277 523      DD NONE,X,NOP,OR,ZA,X,13,X ;R13
0258 001C0DOO      1 524      DEFB NONE+X,NOP+OR+ZA,X#16+13,X
025C          278 526      DD NONE,X,NOP,OR,ZA,X,14,X ;R14
025C 001C0EOO      1 527      DEFB NONE+X,NOP+OR+ZA,X#16+14,X
0260          279 529      DD NONE,X,NOP,OR,ZA,X,15,X ;R15
0260 001C0FOO      1 530      DEFB NONE+X,NOP+OR+ZA,X#16+15,X
0264          280 532      BM R,X,X,STROO1
0264 1C200014      1 533      DEFB 1CH,R+X,X,STROO1/4 ; >>>> STROO1
;::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
0280          282 536      ORG 280H      ;WORD ADDRESS AOH,ENTRY FOR
                                STATE 5
                                ;STATE 5: WAITING FOR ACKNOWLEDGMENT FROM Z80
0280          284 538 ST5000 BPT
0280 00000000      1 539      DEFB 0,0,0,0      ;PATCHABLE B/PT
0284          285 541      BRDY R,X,RDYA,START ;TO START IF PIO
                                OUTPUT NOT READY
0284 1C210000      1 542      DEFB 1CH,R+X+RDYA,0,START/4 ; >>>> START
0288          286 544      DD NONE,POD,RAMF,OR,DZ,12,X,0 ;R12<ACK
                                CODE
0288 015FC000      1 545      DEFB NONE+POD,RAMF+OR+DZ,12#16+X,0
028C          287 547      BM R,X,Z,ST5001 ;TO ST5001 IF NOT 0 (OK)
028C 1C2040AD      1 548      DEFB 1CH,R+X,Z,ST5001/4 ; >>>> ST5001
0290          288 550      DD LA,D,RAMF,OR,DZ,5,X,7 ;LA,R5<7 START
                                CELL FOR ACK TONE
0290 0C5F5007      1 551      DEFB LA+D,RAMF+OR+DZ,5#16+X,7
0294          289 553      DD RO,X,NOP,OR,DZ,X,X,OEOH ;OK TONE CODE
0294 041FOOEO      1 554      DEFB RO+X,NOP+OR+DZ,X#16+X,OEOH
0298          290 556      DD NONE,D,RAMF,OR,DZ,6,X,7 ;R6<7
0298 005F6007      1 557      DEFB NONE+D,RAMF+OR+DZ,6#16+X,7
                                ; EXIT ROUTINE FROM THIS SECTION
029C          292 560 ST5002 DD LA,D,RAMF,OR,DZ,5,X,1 ;LA,R5<1
029C 0C5F5001      1 561      DEFB LA+D,RAMF+OR+DZ,5#16+X,1
02A0          293 563      DD RO,X,NOP,OR,ZA,X,6,X ;BIT/CELL FOR
                                ACK TONE<R6
02A0 041C0600      1 564      DEFB RO+X,NOP+OR+ZA,X#16+6,X

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O2A4	294	566	DD LA,D,RAMF,OR,DZ,5,X,O ;LA,R5<O
O2A4 OC5F5000	1	567	DEFB LA+D,RAMF+OR+DZ,5#16+X,O
O2A8	295	569	DD NONE,D,RAMF,OR,DZ,15,X,O ;R15<O Z80
			FLAG UNBUSY
O2A8 005FF000	1	570	DEFB NONE+D,RAMF+OR+DZ,15#16+X,O
O2AC	296	572	DD RO,X,NOP,OR,DZ,X,X,OCOH ;SET STATE 6
O2AC 041FOOCO	1	573	DEFB RO+X,NOP+OR+DZ,X#16+X,OCOH
O2BO	297	575	BM R,X,X,START ;TO START
O2BO 1C200000	1	576	DEFB 1CH,R+X,X,START/4 ; >>>> START
			:IF ACK CODE NOT OK (O)
O2B4	299	579 ST5001	DD NONE,D,NOP,SUBR,DA,X,12,O ;STATS OF
			R12-1
O2B4 000DOCOO	1	580	DEFB NONE+D,NOP+SUBR+DA,X#16+12,O
O2B8	300	582	BM R,X,Z,ST5003 ;TO ST5003 IF #O IE
			ACK 2
O2B8 1C20402D	1	583	DEFB 1CH,R+X,Z,ST5003/4 ; >>>> ST5003
O2BC	301	585	DD LA,D,RAMF,OR,DZ,5,X,7
O2BC OC5F5007	1	586	DEFB LA+D,RAMF+OR+DZ,5#16+X,7
O2CO	302	588	DD RO,X,NOP,OR,DZ,X,X,88H
O2CO 041FO088	1	589	DEFB RO+X,NOP+OR+DZ,X#16+X,88H
O2C4	303	591	DD LA,D,RAMF,OR,DZ,5,X,6
O2C4 OC5F5006	1	592	DEFB LA+D,RAMF+OR+DZ,5#16+X,6
O2C8	304	594	DD RO,X,NOP,OR,DZ,X,X,88H
O2C8 041FO088	1	595	DEFB RO+X,NOP+OR+DZ,X#16+X,88H
O2CC	305	597	DD LA,D,RAMF,OR,DZ,5,X,5
O2CC OC5F5005	1	598	DEFB LA+D,RAMF+OR+DZ,5#16+X,5
O2DO	306	600	DD RO,X,NOP,OR,DZ,X,X,88H
O2DO 041FO088	1	601	DEFB RO+X,NOP+OR+DZ,X#16+X,88H
O2D4	307	603	DD LA,D,RAMF,OR,DZ,5,X,4
O2D4 OC5F5004	1	604	DEFB LA+D,RAMF+OR+DZ,5#16+X,4
O2D8	308	606	DD RO,X,NOP,OR,DZ,X,X,88H ;ABOVE LOADS
			RAPID BURST CODE
O2D8 041FO088	1	607	DEFB RO+X,NOP+OR+DZ,X#16+X,88H
			FOR PHYSICAL ERROR
O2DC	310	610	DD NONE,D,RAMF,OR,DZ,6,X,5;R6<4 START
			CELL OF BURST

```

O2DC 005F6005      1  611      DEFB NONE+D,RAMF+OR+DZ,6*16+X,4
O2EO                311  613      BM R,X,X,ST5002 ;TO EXIT RTM
O2EO 1C2000A7      1  614      DEFB 1CH,R+X,X,ST5002/4 ; >>>> ST5002
                                ; REMAINDER OF THIS ROUTINE FOLLOWS STATE 1 CODE
                                ;
                                ;::::::::::::::::::::::::::::::::::::::::::
O300                315  619      ORG 300H ;WORD ADDRESS COH, ENTRY FOR
                                STATE 6
                                ;STATE 6: ACKNOWLEDGING TO DEVICE
O300                317  621 ST6000 BPT
O300 00000000      1  622      DEFB 0,0,0,0 ;PATCHABLE B/PT
O304                318  624      BM R,X,TT,START ;TO START IF T=0 IE NOT
                                TIMER CYCLE
O304 1C200100      1  625      DEFB 1CH,R+X,TT,START/4 ; >>>> START
O308                319  627      DD LA,D,RAMF,OR,DZ,5,X,1 ;R5,LA<1
O308 0C5F5001      1  628      DEFB LA+D,RAMF+OR+DZ,5*16+X,1
O30C                320  630      DD NONE,RI,RAMF,OR,DZ,2,X,X ;R2<RAM 1
                                IE BIT/CELL
O30C 025F2000      1  631      DEFB NONE+RI,RAMF+OR+DZ,2*16+X,X
O310                321  633      DD NONE,X,RAMF,OR,ZA,6,2,X ;R6<R2
O310 005C6200      1  634      DEFB NONE+X,RAMF+OR+ZA,6*16+2,X
O314                322  636      DD NONE,D,RAMF,ADD,DA,2,2,10H ;R2<R2+10H
                                NEXT BIT
O314 00452210      1  637      DEFB NONE+D,RAMF+ADD,DA+2*16+2,10H
O318                323  639      BM R,X,F3H,ST6001 ;SKIP IF BIT <=7
O318 1C2008C8      1  640      DEFB 1CH,R+X,F3H,ST6001/4 ; >>>> ST6001
O31C                324  642      DD NONE,D,RAMF,ADD,DA,2,2,81H ;BIT0 NEXT
                                CELL
O31C 00452281      1  643      DEFB NONE+D,RAMF+ADD,DA+2*16+2,81H
O320                325  645 ST6001 DD RO,X,NOP,OR,ZA,X,2,X ;RAM 1<R2 UPDATE
                                BC
O320 041C0200      1  646      DEFB RO+X,NOP+OR+ZA,X*16+2,X
O324                326  648      DD LA,X,NOP,OR,ZA,X,6,X ;LA<R6 IE LA<CELL
                                BEFORE UPDATE
O324 0C1C0600      1  649      DEFB LA+X,NOP+OR+ZA,X*16+6,X
O328                327  651      DD NONE,RI,RAMF,OR,DZ,3,X,X ;R3<BYTE C
O328 025F3000      1  652      DEFB NONE+RI,RAMF+OR+DZ,3*16+X,X

```


032C	328	654	DD E,D,NOP,AND,DA,X,3,80H ;EA<BIT7 OF R3
032C 18250380	1	655	DEFB E+D,NOP+AND+DA,X#16+3,80H
0330	329	657	DD NONE,X,RAMU,OR,ZA,3,3,X ;R3<SHIFT LEFT (R3)
0330 00DC3300	1	658	DEFB NONE+X,RAMU+OR+ZA,3#16+3,X
0334	330	660	DD RO,X,NOP,OR,ZA,X,3,X;RAM(C)<R3 UPDATE WITH SHIFTED VALUE
0334 041C0300	1	661	DEFB RO+X,NOP+OR+ZA,X#16+3,X
0338	331	663	DD LA,D,RAMF,OR,DZ,5,X,0 ;R5,LA<0
0338 0C5F5000	1	664	DEFB LA+D,RAMF+OR+DZ,5#16+X,0
033C	332	666	DD NONE,X,NOP,OR,ZA,X,2,X ;STATS OF R2 (UPDATED BC)
033C 001C0200	1	667	DEFB NONE+X,NOP+OR+ZA,X#16+2,X
0340	333	669	BM R,X,F3L,START ;TO START IF CELL <=7
0340 1C200400	1	670	DEFB 1CH,R+X,F3L,START/4 ; >>>> START
0344	334	672	DD RO,D,RAMF,OR,DZ,1,X,OE0H ;SET STATE 7
0344 045F10E0	1	673	DEFB RO+D,RAMF+OR+DZ,1#16+X,OE0H
0348	335	675	BM R,X,X,START ;TO START
0348 1C200000	1	676	DEFB 1CH,R+X,X,START/4 ; >>>> START
;::			
0380	337	679	ORG 380H ;WORD ADDRESS E0H, ENTRY FOR STATE 7
;STATE 7: CLEARING SUB-CHANNEL FOR NEXT BADGE			
0380	339	681	ST7000 BPT
0380 00000000	1	682	DEFB 0,0,0,0 ;PATCHABLE B/PT
0384	340	684	DD RO,D,NOP,OR,DZ,X,X,OFH ;STATE 0 AND FRESH TIME OUT VALUE
0384 041F000F	1	685	DEFB RO+D,NOP+OR+DZ,X#16+X,OFH
0388	341	687	DD LA,D,RAMF,OR,DZ,5,X,1 ;LA,R5<1
0388 0C5F5001	1	688	DEFB LA+D,RAMF+OR+DZ,5#16+X,1
038C	342	690	DD RO,D,NOP,OR,DZ,X,X,2 ;BIT/CELL BYTE<02H
038C 041F0002	1	691	DEFB RO+D,NOP+OR+DZ,X#16+X,2
0390	343	693	DD NONE,D,RAMF,OR,DZ,4,X,6 ;R4<6
0390 005F4006	1	694	DEFB NONE+D,RAMF+OR+DZ,4#16+X,6

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0394          344 696      DD LA,D,RAMF,OR,DZ,5,X,2 ;LA,R5<2
0394 OC5F5002      1 697      DEFB LA+D,RAMF+OR+DZ,5#16+X,2
0398          345 699 ST7001 DD RO,D,NOP,OR,DZ,X,X,0 ;RAM(C)<0
0398 041F0000      1 700      DEFB RO+D,NOP+OR+DZ,X#16+X,0
039C          346 702      DD LA,D,RAMF,ADD,DA,5,5,1 ;LA,R5<R5+1
039C OC455501      1 703      DEFB LA+D,RAMF+ADD+DA,5#16+5,1
03A0          347 705      DD NONE,D,RAMF,SUBR,DA,4,4,0 ;DECR
                        COUNTER
03A0 004D4400      1 706      DEFB NONE +D,RAMF+SUBR+DA,4#16+4,0
03A4          347 708      BM R,X,Z,ST7001 ;LOOP BACK IF NOT DONE
03A4 1C2040E6      1 709      DEFB 1CH,R+X,Z,ST7001/4 ; >>>> ST7001
03A8          349 711      BM R,X,X,START ;TO START NOW ALL ZERO
03A8 1C200000      1 712      DEFB 1CH,R+X,X,START/4 ; >>>> START
                        ;::::::::::::::::::::::::::::::::::::::::::
                        ;CONTINUATION OF RESET ROUTINE .....
                        ;CAUSES A MASKED SCAN OF ALL S/CHANS TO RESET
                        ;LATCHES ON THE CHANNEL CARDS AFTER POWER ON.
                        ;CODE IS AS NORMAL BASE SCAN.
03AC          355 719 RST003 DD LAE,D,RAMF,OR,DZ,5,X,40H
03AC 145F5040      1 720      DEFB LAE+D,RAMF+OR+DZ,5#16+X,40H
03B0          356 722      DD HA,D,RAMF,ADD,DA,0,0,2
03B0 10450002      1 723      DEFB HA+D,RAMF+ADD+DA,0#16+0,2
03B4          357 725      BM R,X,Z,RST004 ;SKIP IF S/C IS NOT ZERO
03B4 1C2040F1      1 726      DEFB 1CH,R+X,Z,RST004/4; >>>> RST004
03B8          358 728      DD E,D,NOP,OR,DZ,X,X,60H
03B8 181F0060      1 729      DEFB E+D,NOP+OR+DZ,X#16+X,60H
03BC          359 731      DD E,D,NOP,OR,DZ,X,X,40H
03BC 181F0040      1 732      DEFB E+D,NOP+OR+DZ,X#16+X,40H
03C0          360 734      DD NONE,X,NOP,X,X,X,X,X
03C0 00000000      1 735      DEFB NONE+X,NOP+X+X,X#16+X,X
03C4          361 737 RST004 DD LAE,D,RAMF,OR,DZ,5,X,0
03C4 145F5000      1 738      DEFB LAE+D,RAMF+OR+DZ,5#16+X,0
03C8          362 740      BPT
03C8 00000000      1 741      DEFB 0,0,0,0 ;PATCHABLE B/PT
03CC          363 743      BPT
03CC 00000000      1 744      DEFB 0,0,0,0 ;PATCHABLE B/PT

```

O3D0	364	746	BPT
O3D0 00000000	1	747	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3D4	364	749	BPT
O3D4 00000000	1	750	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3D8	366	752	BPT
O3D8 00000000	1	753	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3DC	367	755	BPT
O3DC 00000000	1	756	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3E0	368	758	BPT
O3E0 00000000	1	759	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3E4	369	761	BPT
O3E4 00000000	1	762	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3E8	370	764	BPT
O3E8 00000000	1	765	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3EC	371	767	BPT
O3EC 00000000	1	768	DEFB 0,0,0,0 ;PATCHABLE B/PT
O3FO	372	770	BM X,X,RESET,RSTOO3 ;LOOP UNTIL RESET LINE GOES OFF.
O3FO 1C0080EB	1	771	DEFB 1CH,X+X,RESET,RSTOO3/4 ; >>>> RSTOO3
O3F4	373	773	BM R,X,X,START ;THEN TO START
O3F4 1C200000	1	774	DEFB 1CH,R+X,X,START/4 ; >>>> START
O3F8	374	776	END

APPENDIX II

PCI MOSTEK ROM LOADER

MOSTEK MACRO-80 ASSEMBLER V2.2

LOC OBJ.CODE

SIMT-NR SOURCE-SIMT PASS 2 RM25JI RM25JI RM25JI REL

1 TITLE PCI MOSTEK ROM LOADER

; :::: ::::

;

; MACROS

5 CDELAY MACRO

;DELAY APPR 1 AWX IF SWO ON

1 6 IN A,(P101+2)

2 7 AND 1

3 8 JR Z,+17

4 9 LD B,4

5 10 OR A

6 11 LD HL,0

7 12 LD DE,1

8 13 ADC HL,DE

9 14 JR NZ,-2

10 15 DJNZ -4

11 16 MEND

17 DISP MACRO #N

1 18 LD A,#N

2 19 OUT (P101),A

3 20 MEND

21 CSUM MACRO

1 22 XOR A

2 23 LD HL,2047

3 24 LD DE,1

4 25 ADD A,(IX)

5 26 INC IX

6 27 OR A

7 28 SBC HL,DE

8 29 JR NZ,-8

9 30 SUB (IX)

10 31 INC IX

11 32 MEND

```

33 HALTNZ MACRO
1 34 JR Z,+3
2 35 HALT
3 36 MEND
37 OUTN MACRO #P, #N
1 38 LD A,#N
2 39 OUT (#P),A
3 40 MEND
;
=0050 42 P101 EQU 5CH
;
0000'F3 44 START DI
0001 45 OUTN P101,OFFH
0001 3EFF 1 46 LD A,OFFH
0003 D350 2 47 OUT (P101),A
3 48 MEND
0005 D352 46 49 OUT (P101+2),A
0007 47 50 OUTN P101+1,OCFH
0007 3ECF 1 51 LD A,OCFH
0009 D351 2 52 OUT (P101+1),A
3 53 MEND
000B 48 54 OUTN P101+1,O
000B 3E00 1 55 LD A,O
000D D351 2 56 OUT (P101+1),A
3 57 MEND
000F 49 58 OUTN P101+3,OCFH
000F 3ECF 1 59 LD A,OCFH
0011 D353 2 60 OUT (P101+3),A
3 61 MEND
0013 50 62 OUTN P101+3,-1
0013 3EFF 1 63 LD A,-1
0015 D353 2 64 OUT (P101+3),A
3 65 MEND
0017 DD210000 51 66 LD 1X,0

```

001B	52	67	DISP 0
001B 3E00	1	68	LD A,0
001D D350	2	69	OUT (P101),A
	3	70	MEND
001F	53	71	CSUM ROM 0 — LOADER ITSELF
001F AF	1	72	XOR A
0020 21FF07	2	73	LD HL,2047
0023 110100	3	74	LD DE,1
0026 DD8600	4	75	ADD A,(IX)
0029 DD23	5	76	INC IX
002B B7	6	77	DR A
002C ED52	7	78	SBC HL,DE
002E 20F6	8	79	JR NZ,-8
0030 DD9600	9	80	SUB (IX)
0033 DD23	10	81	INC IX
	11	82	MEND
0035	54	83	HALINZ
0035 2801	1	84	JR Z,+3
0037 76	2	85	HALT
	3	86	MEND
0038	55	87	DISP 1
0038 3E01	1	88	LD A,1
003A D350	2	89	OUT (P101),A
	3	90	MEND
003C	56	91	CSUM ROM 1 — F/G Z80 CODE
003C AF	1	92	XOR A
003D 21FF07	2	93	LD HL,2047
0040 110100	3	94	LD DE,1
0043 DD8600	4	95	ADD A,(IX)
0046 DD23	5	96	INC IX
0048 B7	6	97	OR A
0049 ED52	7	98	SBC HL,DE
004B 20F6	8	99	JR NZ,-8
004D DD9600	9	100	SUB (IX)

0050 DD23	10 101	INC IX
	11 102	MEND
0052	57 103	HALTIZ
0052 2801	1 104	JR Z,+3
0054 76	2 105	HALT
	3 106	MEND
0055	58 107	DISP 2
0055 3E02	1 108	LD A,2
0057 D350	2 109	OUT (P101),A
	3 110	MEND
0059	59 111	CSUM ROM 2 -- B/G Z80 CODE
0059 AF	1 112	XOR A
005A 21FF07	2 113	LD HL,2047
005D 110100	3 114	LD DE,1
0060 DD8600	4 115	ADD A,(IX)
0063 DD23	5 116	INC IX
0065 B7	6 117	OR A
0066 ED52	7 118	SBC HL,DE
0068 20F6	8 119	JR NZ,-8
006A DD9600	9 120	SUB (IX)
006D DD23	10 121	INC IX
	11 122	MEND
006F	60 123	HALTIZ
006F 2801	1 124	JR Z,+3
0071 76	2 125	HALT
	3 126	MEND
0072	61 127	DISP 3
0072 3E03	1 128	LD A,3
0074 D350	2 129	OUT (P101),A
	3 130	MEND
0076	62 131	CSUM ROM 3 -- MICRO-CODE
0076 AF	1 132	XOR A
0077 21FF07	2 133	LD HL,2047
007A 110100	3 134	LD DE,1

```

007D DD8600      4 135      ADD A,(IX)
0080 DD23        5 136      INC IX
0082 B7          6 137      OR A
0083 ED52        7 138      SBC HL,DE
0085 20F6        8 139      JR NZ,-8
0087 DD9600      9 140      SUB (IX)
00BA DD23       10 141      INC IX
                   11 142      MEND
00BC             63 143      HALT
00BC 2801        1 144      JR Z,+3
00BE 76          2 145      HALT
                   3 146      MEND
                   ; END OF ROM CHECKSUM VERIFICATION
00BF             65 148      DISP 10H
00BF 3E10        1 149      LD A,10H
0091 D350        2 150      OUT (P101),A
                   3 151      MEND
0093 DD210040    66 152      LD IX,4000H
0097 210080      67 153      LD HL,8000H
009A 110100      68 154      LD DE,1
009D 3E01        69 155      LD A,1
009F'CB27       70 156 L1039 SLA A
00A1 FE80        71 157      CP 80H
00A3 2002        72 158      JR NZ,L1040-1
00A5 3E01        73 159      LD A,1
00A7'DD7700     74 160 L1040 LD (IX),A
00AA DD23        75 161      INC IX
00AC B7          76 162      OR A
00AD ED52        77 163      SBC HL,DE
00AF 20EE        78 164      JR NZ,L1039-1
                   ;
00B1 DD210040    80 166      LD IX,4000H
00B5 210080      81 167      LD HL,8000H
00B8 3E01        82 168      LD A,1

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00BA'CB27	83	169	L1041	SLA	A
00BC FE80	84	170		CP	80H
00BE 2002	85	171		JR	NZ,L1042-4
00C0 3E01	86	172		LD	A,1
00C2'DDE00	87	173	L1042	CP	(IX)
00C5	88	174		HALT	NZ
00C5 2801	1	175		JR	Z,+3
00C7 76	2	176		HALT	
	3	177		MEND	
00C8 DD23	89	178		INC	IX
00CA B7	90	179		OR	A
00CB ED52	91	180		SBC	HL,DE
00CD 20EB	92	181		JR	NZ,L1041-4
; END OF RAM TEST					
00CF	94	183		DISP	21H
00CF 3E21	1	184		LD	A,21H
00D1 D350	2	185		OUT	(P101),A
	3	186		MEND	
00D3 110040	95	187		LD	DE,4000H
00D6 210008	96	188		LD	HL,800H
00D9 010008	97	189		LD	BC,800H
00DC EDE0	98	190		LDIR	;COPY F/G ROM TO RAM
00DE DD210040	99	191		LD	IX,4000H
00E2	100	192		CSUM	
00E2 AF	1	193		XOR	A
00E3 21FF07	2	194		LD	HL,2047

00E6	110100	3	195	LD	DE,1	
00E9	DD8600	4	196	ADD	A,(IX)	
00EC	DD23	5	197	INC	IX	
00EE	B7	6	198	OR	A	
00EF	ED52	7	199	SBC	HL,DE	
00F1	20F6	8	200	JR	NZ,-8	
00F3	DD9600	9	201	SUB	(IX)	
00F6	DD23	10	202	INC	IX	
		11	203	MEND		
00F8		101	204	HALT		
00F8	2801	1	205	JR	Z,+3	
00FA	76	2	206	HALT		
		3	207	MEND		
00FB		102	208	DISP	22H	
00FB	3E22	1	209	LD	A,22H	
00FD	D350	2	210	OUT	(P101),A	
		3	211	MEND		
00FF	110048	103	212	LD	DE,4800H	
0102	210010	104	213	LD	HL,1000H	
0105	010008	105	214	LD	BC,800H	
0108	EDB0	106	215	LDIR		;COPY B/G ROM TO RAM
010A		107	216	CSUM		
010A	AF	1	217	XOR	A	
010B	21FF07	2	218	LD	HL,2047	
010E	110100	3	219	LD	DE,1	
0111	DD8600	4	220	ADD	A,(IX)	

0114	DD23	5	221	INC	IX	
0116	B7	6	222	OR	A	
0117	ED52	7	223	SBC	HL,DE	
0119	20F6	8	224	JR	NZ,-8	
011B	DD9600	9	225	SUB	(IX)	
011E	DD23	10	226	INC	IX	
		11	227	MEND		
0120		108	228	HALTINZ		
0120	2801	1	229	JR	Z,+3	
0122	76	2	230	HALT		
		3	231	MEND		
0123		109	232	DISP	23H	
0123	3E23	1	233	ID	A,23H	
0125	D350	2	234	OUT	(P101),A	
		3	235	MEND		
0127	110050	110	236	ID	DE,5000H	
012A	210018	111	237	ID	HL,1800H	
012D	01000B	112	238	ID	BC,800H	
0130	EDE0	113	239	IDIR		;COPY MICRO-CODE TO RAM
0132		114	240	CSUM		
0132	AF	1	241	XOR	A	
0133	21FF07	2	242	ID	HL,2047	
0136	110100	3	243	ID	DE,1	
0139	DD8600	4	244	ADD	A,(IX)	
013C	DD23	5	245	INC	IX	
013E	B7	6	246	OR	A	
013F	ED52	7	247	SBC	HL,DE	
0141	20F6	8	248	JR	NZ,-8	
0143	DD9600	9	249	SUB	(IX)	
0146	DD23	10	250	INC	IX	
		11	251	MEND		
014B		115	252	HALTINZ		
0148	2801	1	253	JR	Z,+3	
014A	76	2	254	HALT		
		3	255	MEND		

;END OF ROM-RAM COPIES AND TESTS IN RAM

[illegible]

APPENDIX III

PCI MOSTEK Z80 NMUX PROGRAM MOSTEK MACRO-80 ASSEMBLER V2.2
 LOC OBJ CODE STMT-NR SOURCE-STMT PASS2PCIZ12 PCIZ12 PCIZ12 REL

```

1      TITLE PCI MOSTEK Z80 NMUX PROGRAM
      ; ::::      ::::
      ;;; LIST 0
      ; MACROS .....
5 WAIT  MACRO #LED, #SW
      ; DISPLAY #LED AND LOOP IF (SWITCH& #SW)=NZ !!
2  7      LD  A, #LED
3  8      OUT (P101),A
4  9      IN  A,(P101+2)
5 10      AND #SW
6 11      JR   NZ,-4
7 12      MEND
13 LOOP MACRO #AD, #LED, #SW
      ;DISPLAY #LED, GOTO #AD IF (SWITCH& #SW)=NZ !
2 15      LD  A, #LED
3 16      OUT (P101),A
4 17      IN  A,(P101+2)
5 18      AND #SW
6 19      JP   NX, #AD
7 20      MEND
21 BPT  MACRO
1 22      JP  $+23 ;PATCHABLE BREAKPOINT
2 23      DEFB 0,0,0,0,0,0,0,0,0,0
3 24      DEFB 0,0,0,0,0,0,0,0,0,0
4 25      MEND
26 INCW MACRO #ADDR      ;INCREMENT L-H WORD AT ADDRESS
                        S
1 27      PUSH HL
2 28      LD   HL,( ADDR) -
3 29      INC  HL
4 30      LD   ($ADDR),HL
5 31      POP  HL

```

```

6 32      MEND
      33 DECW MACRO #ADDR ;DECREMENT L-H WORD AT ADDRESS
                        S
1 34      PUSH HL
2 35      LD HL,(#ADDR)
3 36      DEC HL
4 37      LD (#ADDR),HL
5 38      POP HL
6 39      MEND
      40 TERM MACRO #A :HALT WITH CODE IN LHS
1 41      LD A,#A
2 42      OUT (P10),A
3 43      HALT
4 44      JR -1
5 45      MEND
      46 OUTN MACRO #P, #N
1 47      LD A, #N
2 48      OUT (#P),A
3 49      MEND
      50 FILL MACRO #FROM, #TO, #WITH
      :FILL FROM #FROM TO #TO WITH #WITH
2 52      MLOCAL LI
3 53      MIF (.RES. #TO- #FROM) < 2 THEN LI
4 54      LD A, #WITH
5 55      LD DE, -#FROM
6 56      LD (DE),A
7 57      LD H,D
8 58      LD L,E
9 59      INC DE
10 60      LD BC,.RES. #TO- #FROM
11 61      LDIR
12 62      MEXIT
13 63 LI MERROR FILL STRING TOO SHORT
14 64      MEND
      ;
66      LIST 1

```

```

67          CLIST 0
;
=007C      69 CTC    EQU  7CH    ;PORT ADDRESSES
=0060      70 SIO    EQU  60H
=0050      71 PIO    EQU  50H
=0050      72 P101   EQU  50H
=0054      73 P102   EQU  54H
=0054      74 P102A  EQU  54H
=0056      75 P102B  EQU  56H
;
=F2A4      77 MENLIS EQU  0F2A4H ;MDX DEVSYS ENTRY PT.
;
=6000      79 TRANST EQU  6000H  ;START OF TRANS AREA
=BFFF      80 TRANEN EQU  0BFFFH  ;END
=0C00      81 SLOTS  EQU  0C00H   ;3K FOR MOSTEK
;FOLLOWING MUST RETAIN TRAILING ZEROS
=5800      83 SUBCHS EQU  5800H   ;START OF S/C TABLE
=0008      84 PARWKL EQU   8      ;LENGTH OF PARITY WORK AREA
=4100      85 VARST  EQU  4100H   ;START OF VARIABLES AND ORIGI
N-
; -OF DIAGNOSTIC PAGE.
;
4000      88          ORG  04000H
4000'C3A742' 89 ORIGIN JP   START  ;SKIP OVER VECTORS ETC.
4003 434F5059 90          DEFM 'COPYRIGHT P.C.I. LIMITED 1982'
52494748
5420502E
432E492E
204C494D
49544544
20313938
32
=4020'      91 CONT  EQU  $      ;MUST BE MOD 16 BOUNDARY
4020'3C40'  93 CTCVEC DEFW TRAP  ;TO TRAPCELL
4022 A4F2    94          DEFW MINLIS ;MINIMUM LISTENER MDX DEVSYS

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4024 3C40'	95	DEFW TRAP	
4026 4D44'	96	DEFW ONESEC	;ONE SECOND TIMER
			;
4028' 3C40'	98	SIOVEC DEFW TRAP	;SIO CH B XMIT BUF EMPTY
402A 3C40'	99	DEFW TRAP	;EXIT STATUS CHANGE
402C 3C40'	100	DEFW TRAP	;RECV CHAR AVAILABLE
402E 3C40'	101	DEFW TRAP	;SPEC RECV COND
			; ABOVE TRAPS SINCE PORT B UNUSED
4030 DF44'	103	DEFW SIATBE	;CH A
4032 3C40'	104	DEFW TRAP	;EXIT STATUS, NOT USED

0094800

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4034 2544'      105      DEFN STAREC
4034 2544'      106      DEFN STAREC
; PORT A OF PIO 2
403B' 2545'      108 FIAYEC DEFN PIADUT ;PIO BIDIRECT OUT
403A 3545'      109      DEFN PIAIN ;IN
;
403C'          111 TRAP TERM OEEH ;TERMINAL ERROR 1111
403C 3EEF      1 112      LD A,OEEH
403E D350      2 113      OUT (PIO),A
4040 76        3 114      HALT
4041 1BFD      4 115      JR -1
;
;CONSTANTS .....
4043'000C      114 119 NSLDTS DEFN SLOTS ;3K SLOTS IN MOSTEK
; COLUMNS IN FOLL ARRAY ARE 0123=CURRENT STATE
; ROWS ARE LOG,OP,BUND,RESVB,LDG(BIT29)
; CELLS ARE CURR-STATE (7,6), LOGERR (5), NEXTSTATE (1
;0)
=4045' 118 123 STABLE EQU 4
4045 0140B0C0 119 124 DEFN 00000001B,01000000B,10000000B,11000000B
4049 2042B2E3 120 125 DEFN 00100000B,01000010B,10000010B,11100011B
404D 2061B3C3 121 126 DEFN 00100000B,01100001B,10000011B,11000011B
4051 2061A2E3 122 127 DEFN 00100000B,01100001B,10100010B,11100011B
4055 0040B0C0 123 128 DEFN 00000000B,01000000B,10000000B,11000000B
; ECC BIT MASKS
4059'55555555 125 130 MASK0 DEFN 01010101B,01010101B,01010101B,01010101B
405D'66666666 126 131 MASK1 DEFN 01100110B,01100110B,01100110B,01100110B
4061'78787878 127 132 MASK2 DEFN 01111000B,01111000B,01111000B,01111000B
4065'7F807F80 128 133 MASK3 DEFN 01111111B,10000000B,01111111B,10000000B
4069'7FFF8000 129 134 MASK4 DEFN 01111111B,11111111B,10000000B,00000000B
;BITS 33222222 22221111 11111100 00000000
; 10987654 32109876 54321098 76543210
;
=406D' 133 138 BOTSTK EQU 4
;
;VARIABLES .....
4100 136 141 ORG VARST
4100 137 142 DEFS 64 ;TOP 32 WORDS OF STACK
=4140' 138 143 TOPSTK EQU 4
4140'00 139 144 TYPE DEFN 0 ;WORK-AREAS FOR LOGICAL ERR R
;TN (BADGE TYPE)
4141'00 140 145 ESTATE DEFN 0 ;CURRENT STATE OF DID
4142'00 141 146 CELL DEFN 0 ;CONTENTS OF TRANSITION TABLE
;CELL
4143'00 142 147 SUBCHA DEFN 0 ;ACTIVE SUB-CHANNEL
4144'00 143 148 ACKCB DEFN 0 ;ACKNOWLEDGE CODE
4145'00000000 144 149 CLCCL NTF 0,C,0,0 ;32-BIT RELATIVE SECS
4149'0000 145 150 NMSTA DEFN 0 ;NRUY STATUS ??
414B'0000 146 151 LSTRND DEFN 0 ;LAST TRANS IN MEM
;!! NOTE TRANS NOS START AT 1 !!
414D'000C 148 153 NLEFT DEFN SLOTS ;NO OF SLOTS LEFT
414F'0000 149 154 HTRAN DEFN 0 ;HIGHEST TRN SENT
4151'0000 150 155 NREADS DEFN 0 ;NO OF READS
4153'0000 151 156 NPERIO DEFN 0 ;IFNIEFS DUE TO TIMEOUT
4155'0000 152 157 NPEINI DEFN 0 ;# OF INITIAL PARITY/ECC ERRS
4157'0000 153 158 NPERCO DEFN 0 ;NERRORS CORR BY ECC
4159'0000 154 159 NGOOD DEFN 0 ;# OF GOOD BLOCKS

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0094800

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415E'0000 155 160 NPHYER DEFW 0 ;1 OF PHYS ERRS
415D'0000 156 161 NLOGER DEFW 0 ;LOGICAL ERRORS
;
415F'0000 158 163 NGHIN DEFW 0 ;GOOD HOST INBLOCKS
4161'0000 159 164 NBNIN DEFW 0 ;BAD HOST INBLOCKS
4163'0000 160 165 NHDUT DEFW 0 ;HOST OUTBLOCKS
;
;MICRO-SEQUENCER INBLOCK AND FLAG ..
4165'00 163 166 MSIFLG DEFB 0 ;0-FREE,1-BUSY.F/6,2-BUSY.B/6
4166'00 164 169 MSIBCT DEFB 0 ;BYTE COUNTER
4167'00 165 170 MSISCH DEFB 0 ;SUB-CHANNEL
4168'00000000 166 171 MSDATA DEFB 0,0,0,0,0,0,0,0 ;DATA AS IN MSED BUFFER
00000000
;
;MICRO-SEQUENCER OUTBLOCK AND FLAG ..
4170'00 169 174 MSOFLG DEFB 0 ;0-FREE,1-BUSY.B/6,2-BUSY.F/6
4171'00 170 175 MSOACK DEFB 0 ;ACK CODE: 0-GOOD,1-PHYS,2-L
;
;HOST INBLOCK AND FLAG ..
4172'00 173 178 HTIFLG DEFB 0 ;0-FREE,1-BUSY.F/6,2-BUSY.B/6
4173'00 174 179 HTIBCT DEFB 0 ;BYTE COUNTER
4174'0000 175 180 HTITYP DEFW 0 ;TRANS TYPE:-1=FULL RESET,1=0
;D RESET,0=TRANS REQUEST
4176'0000 176 181 HTIPRT DEFW 0 ;PORT FOR T1,30564 FOR T-1,0
;FOR T0
4178'00000000 177 182 HTITIM DEFB 0,0,0,0 ;TIME IN ABSOLUTE SECONDS
417C'0000 178 183 HTIS DEFW 0
417E'0000 179 184 HTITMD DEFW 0 ;TRANSD REQUESTED
4180'0000 180 185 HTI7 DEFW 0
4182'0000 181 186 HTI8 DEFW 0
4184'0000 182 187 HTI9 DEFW 0
4186'0000 183 188 HTIHD DEFW 0 ;HI WORD OF SIMULATED DATA
4188'0000 184 189 HTILD DEFW 0 ;LO WORD ****
418A'0000 185 190 HTIJ2 DEFW 0
418C'0000 186 191 HTIJ3 DEFW 0
418E'0000 187 192 HTIJ4 DEFW 0
4190'0000 188 193 HTICK1 DEFW 0 ;CHECKSUM 1
4192'0000 189 194 HTICK2 DEFW 0 ;CHECKSUM 2
;
;HOST OUTBLOCK AND FLAG ..
4194'00 192 197 HTOFLG DEFB 0 ;0-FREE,1-BUSY.B/6,2-BUSY.F/6
4195'00 193 198 HTOBCT DEFB 0 ;BYTE COUNTER
4196'0101 194 199 HTOSER DEFB 1,1 ;NMI SERIAL NO,NMI UNIT1
4198'0000 195 200 HTODJD DEFW 0 ;010 PORT NO DR -1 IF NOT A T
;RANS
419A'00000000 196 201 HTD1M DEFB 0,0,0,0 ;TIME
419E'0000 197 202 HTDHS DEFW 0 ;T11JS TRANS
41A0'0000 198 203 HTDLTM DEFW 0 ;LAST IN MEMORY
41A2'0000 199 204 HTDIFS DEFW 0 ;NO OF FREE SLOTS
41A4'0000 200 205 HTDMS1 DEFW 0 ;NMI STATUS 1
41A6'0000 201 206 HTDMS2 DEFW 0 ;NMI STATUS 2
41A8'0000 202 207 HTDWD DEFW 0 ;HI WORD OF DATA
41AA'0000 203 208 HTDLD DEFW 0 ;LO DATA
41AC'0000 204 209 HTDERC DEFW 0 ;ERROR CODE
41AE'0000 205 210 HTDRS1 DEFW 0 ;RESERVED 1
41B0'0000 206 211 HTDRS2 DEFW 0 ;RESERVED 2

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0094800

41B2'0000	207	212	HTOCK1	DEFW 0	;CHECKSUM 1
41B4'0000	208	213	HTOCK2	DEFW 0	;CHECKSUM 2
41B6'0000	210	215	STAI5T	DEFB 0,0	;SID IN-STATUS RO/I
41B8'0000	211	216	STADST	DEFB 0,0	;SID OUT-STATUS
41BA'0000	212	217	INCK1	DEFW 0	;CALCULATED IN-CHECKSUM
41BC'0000	213	218	INCK2	DEFW 0	; DITTD
41BE'0000	214	219	STARCT	DEFW 0	;ENTRIES TO SID RECV RTN
41C0'0000	215	220	STATCT	DEFW 0	;ENTRIES TO SID TRAN RTN
41C2'0000	216	221	PIAICT	DEFW 0	;ENTRIES TO PID IN RTN
41C4'0000	217	222	PIAOCCT	DEFW 0	;ENTRIES TO PID OUT RTN
41C6'	218	223	PARWK	DEFS PARWKL	;DETAILS OF PARITY CHECKS
41CE'	219	224	CLKWK	DEFS 4	;CLOCK WORK AREA FOR TIME OF
					HTD
41D2'	220	225	TRANWK	DEFS 8	;WORK AREA FOR COPY OF TRANS
41DA'	221	226	TRXTWK	DEFS 4	;WORK AREA FOR TIME PART OF T
					RANS

41DE' 223 228 ENDVAR EQU 4

;SUBROUTINES

41DE'3EFS	227	232	SOLD	LD A,0F5H	;PART OF MICRO-CODE LOADER
41E0 D356	228	233		OUT (P102B),A	
41E2 79	229	234		LD A,C	
41E3 0C	230	235		INC C	
41E4 D354	231	236		OUT (P102A),A	
41E6 C5	232	237		PUSH BC	
41E7 0604	233	238		LD B,4	
41E9'3EFO	234	239	SQ2	LD A,0F0H	
41EB 80	235	240		OR B	
41EC D356	236	241		OUT (P102B),A	
41EE 7E	237	242		LD A,(HL)	
41EF 23	238	243		INC HL	
41F0 D354	239	244		OUT (P102A),A	
41F2 10F5	240	245		DJNZ SQ2-4	
41F4 C1	241	246		POP BC	
41F5 DB56	242	247		IN A,(P102B)	
41F7 EED0	243	248		AND 0D0H	
41F9 D356	244	249		OUT (P102B),A	
41FB F620	245	250		OR 20H	
41FD D356	246	251		OUT (P102B),A	
41FF C9	247	252		RET	

4200' 249 254 CHKSUM EQU 4 ;CALCULATE CHECKSUM FOR
 ; -HOST MESSAGE BLOCK. HL->START OF BLOCK
 ; - DESTROYS F,E,D,E,H,L.

4200 DDE5	252	257		PUSH IX	
4202 FDE5	253	258		PUSH IX	
4204 060E	254	259		LD B,14	
4206 DD210000	255	260		LD IX,0.	
420A FD21C000	256	261		LD IX,0	
420L 56	257	262	CHKSUM	LD D,(HL)	
420F 23	258	263		INC HL	
4210 5E	259	264		LD E,(HL)	
4211 23	260	265		INC HL	
4212 DD19	261	266		ADD IX,DE	;ADD TO IX

0094800

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4214 FD19      262 267      ADD 1Y,DE      ;ADD 1C 1Y
4216 FD29      263 268      ADD 1Y,1Y      ;SHIFT 1Y LEFT INTO CARRY
4218 3002      264 269      JR  AC,CHKS1-8
421A FD23      265 270      INC 1Y      ;ROTATE CARRY INTO LSB
421C DDE5      266 271 CHKS1 PUSH 1X
421E D1        267 272      POP DE
421F 21BA41'   268 273      LD HL,1NCK1
4222 72        269 274      LD (HL),D
4223 23        270 275      INC HL
4224 73        271 276      LD (HL),E
4225 23        272 277      INC HL
4226 FDE5      273 278      PUSH 1Y
4228 D1        274 279      POP DE
4229 72        275 280      LD (HL),D
422A 23        276 281      INC HL
422B 73        277 282      LD (HL),E
422C FDE1      278 283      POP 1Y
422E DDE1      279 284      POP 1X
4230 C9        280 285      RET

;
=4231' 282 287 ECC EQU 8      ;CHECK ONE ECC BIT UNDER MASK
; -POINTED TO BY HL
; RETURN A=1 IF 32-BIT PARITY UNDER MASK IS EVEN,
; ELSE A=0.
4231 C5        286 291      PUSH BC
4232 D5        287 292      PUSH DE
4233 0E00      288 293      LD C,0
4235 0604      289 294      LD B,4
4237 116A41'   290 295      LD DE,MSDATA+2
423A 1A        291 296 ECC1 LD A,(DE)
423B A6        292 297      AND (HL)
423C 23        293 298      INC HL
423D 13        294 299      INC DE
423E EA4242'   295 300      JP PE,ECC2
4241 0C        296 301      INC C      ;C COUNTS BYTES WITH ODD PARITY
4242 10F6      297 302 ECC2 DJNZ ECC1-8
4244 79        298 303      LD A,C
4245 E601      299 304      AND 1
4247 EE01      300 305      XOR 1
4249 D1        301 306      POP DE
424A C1        302 307      POP BC
424B C9        303 308      RET

;
=424C' 305 310 HTDCHM EQU 8      ;CALC AND INSERT HOST OUT-BLD CK CHECKSUM
424C 219641'   306 311      LD HL,HTDCHM
424F CD0942'   307 312      CALL CHXSUM
4252 21BA41'   308 313      LD HL,1NCK1
4255 11B241'   309 314      LD DE,HTDCK1
425B 010400    310 315      LD BC,4
425B EDB0      311 316      LDIR
425D C9        312 317      RET

;
=425E' 314 319 HTDFF EQU 8      ;FORMAT BASIC HTD BLOCK
425E FDE5      315 320      PUSH 1Y
4260 21FFFF    316 321      LD HL,-1

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4263 255E41'	317	322	LD	(HDECI),HL
4264 1221E41'	318	323	LD	IX,HDECI
426A 244F41'	319	324	LD	HL,(HINTER)
426B 11743E	320	325	LD	(IX+6),H
4270 167509	321	326	LD	(IX+9),L
4273 119A41'	322	327	LD	DE,HTDTIM
427A 217B41'	323	328	LD	HL,HTJTIM
4279 016400	324	329	LD	BC,A
427C F3	325	330	DI	
427D ED80	326	331	LDIR	
427F 2A4541'	327	332	LD	HL,(LSTAND)
4282 FD740A	328	333	LD	(IX+10),H
4285 FD750B	329	334	LD	(IX,+11),L
428B 2A4D41'	330	335	LD	HL,(KLEFT)
428B FD740C	331	336	LD	(IX+12),H
428E FD750D	332	337	LD	(IX+13),L
4291 3A4D41'	333	338	LD	A,(HIDERC+1) ;SAVE ERROR CODE
4294 4F	334	339	LD	C,A
4295 21A441'	335	340	LD	HL,HTDKSI
429B AF	336	341	XOR	A
4299 0612	337	342	LD	B,1B
429B*77	338	343	LD	(HL),A
429C 23	339	344	INC	HL
429D 10FC	340	345	DJNZ	HTOF1-4 ;ZERO REST
429F 79	341	346	LD	A,C
42A0 32AD41'	342	347	LD	(HTDERC+1),A
42A3 FDE1	343	348	POP	IX
42A5 FB	344	349	EI	
42A6 C9	345	350	RET	

;				
;				
=42A7'	348	353	START	EDU 4
42A7 F3	349	354	DJ	
42A8 ED5E	350	355	IM	2 ;Z80 INTERRUPT MODE
42AA 210040'	351	356	LD	HL,DRIGIN
42AD 7C	352	357	LD	A,H
42AE ED47	353	358	LD	I,A ;SET VECTOR PAGE TO 40H
42B0 334041'	354	359	LD	SP,TOPSTK ;INIT SP
42B3	355	360	FILL	BDSTK,ENDVAR-1,0
42B3 3E00	4	361	LD	A,0
42B5 116D40'	5	365	LD	DE,BDSTK
42B8 12	6	366	LD	(DE),A
42E9 62	7	367	LD	H,D
42BA 6B	8	368	LD	L,E
42BB 13	9	369	INC	DE
42BC 017001	10	370	LD	BC,.RES.ENDVAR-1-BDSTK
42BF ED80	11	371	LDIR	
42C1	356	373	FILL	PARWK,PARWK+PARWKL-1,0
42C1 3E00	4	377	LD	A,0
42C3 11E641'	5	378	LD	DE,PARWK
42C6 12	6	379	LD	(DE),A
42C7 62	7	380	LD	H,D
42C8 6B	8	381	LD	L,E
42C9 13	9	382	INC	DE
42CA 010700	10	383	LD	BC,.RES.PARWK+PARWKL-1-PARWK
42CB ED80	11	384	LDIR	
42CF	357	386	FILL	SUBCHS,TRANEN,0

42CF 3E00	4	390	LD A,0
42D1 110058	5	391	LD DE,SUBCHS
42D4 12	6	392	LD IDE1,A
42D5 62	7	393	LD H,0
42D6 6B	8	394	LD L,E
42D7 13	9	395	INC DE
42D8 01FF67	10	396	LD BC,.RES.TRANEN-SUBCHS
42D9 EDB0	11	397	LDIR
42DD DD21C641'	358	399	LD J1,PARWK ;STAYS CONSTANT ALWAYS
;			
42E1 212040'	360	401	LD HL,CTEVEC
42E4 7D	361	402	LD A,L
42E5 D37C	362	403	OUT (CTC1),A ;JNT VECTOR
42E7	363	404	OUTX CTC+3,0D7H ;CTC3 COUNT & ENBL
42E7 3ED7	1	405	LD A,0D7H
42E9 D37F	2	406	OUT (CTC+3),A
42EB	364	408	OUTX CTC+3,5DH ;CTC3 T/C 93
42EB 3E5D	1	409	LD A,5DH
42ED D37F	2	410	OUT (CTC+3),A
42EF	365	412	OUTX CTC+2,37H ;CTC2 TIMER P/S 254
42EF 3E37	1	413	LD A,37H
42F1 D37E	2	414	OUT (CTC+2),A
42F3	366	416	OUTX CTC+2,69H ;CTC2 T/C 105
42F3 3E69	1	417	LD A,69H
42F5 D37E	2	418	OUT (CTC+2),A
42F7	367	420	BPT
42F7 C30E43	1	421	JP 1+23 ;PATCHABLE BREAKPOINT
42FA 00000000	2	422	DEFB 0,0,0,0,0,0,0,0,0
00000000			
0000			
4304 00000000	3	423	DEFB 0,0,0,0,0,0,0,0,0
00000000			
0000			
;			
430E	369	426	OUTX P101,OFFH ;SET ALL OUTPUTS HI
430E 3EFF	1	427	LD A,OFFH
4310 D350	2	428	OUT (P101),A
4312 D352	370	430	OUT (P101+2),A
4314 D354	371	431	OUT (P102),A
4316 D356	372	432	OUT (P102+2),A
4318	373	433	OUTX P101+1,0CFH ;CONTROL
4318 3ECF	1	434	LD A,0CFH
431A D351	2	435	OUT (P101+1),A
431C	374	437	OUTX P101+1,0 ;OUTPUT (1A)
431C 3E00	1	438	LD A,0
431E D351	2	439	OUT (P101+1),A
4320	375	441	OUTX P101+3,0CFH ;CONTROL
4320 3ECF	1	442	LD A,0CFH
4322 D353	2	443	OUT (P101+3),A
4324	376	445	OUTX P101+3,OFFH ;INPUT (1B)
4324 3EFF	1	446	LD A,OFFH
4326 D353	2	447	OUT (P101+3),A
4328	377	449	OUTX P102+1,EFH ;BIDIRECTIONAL (2A)
4328 3EBF	1	450	LD A,BFH
432A D355	2	451	OUT (P102+1),A
432C	378	453	OUTX P102+3,0CFH ;CONTROL
432C 3ECF	1	454	LD A,0CFH

0094800

432E D357	2	455	OUT (P102+3),A
4330	379	457	OUTK P102+3,0 ;OUTFJT (28)
4330 3E00	1	458	LD A,0
4332 D357	2	459	OUT (P102+3),A
4334 213840'	380	461	LD HL,PIAVEC
4337 7D	381	462	LD A,L
4338 D355	382	463	OUT (P102+1),A ;OUT VECTOR PORT A
433A 3C	383	464	JMC A
433B 3C	384	465	JMC A
433E D357	385	466	OUT (P102+3),A ;IN VECTOR PORT B
433E	386	467	OUTK P102+1,87H ;ENBL INT PORT A
433E 3E87	1	468	LD A,87H
4340 D355	2	469	OUT (P102+1),A
4342	387	471	OUTK P102+3,97H ;ENBL B & MASK FOLLOWS
4342 3E97	1	472	LD A,97H
4344 D357	2	473	OUT (P102+3),A
4346	388	475	OUTK P102+3,0FFH ;ALL MASKED OFF
4346 3EFF	1	476	LD A,0FFH
4348 D357	2	477	OUT (P102+3),A
434A	389	479	BPT
434A C36143	1	480	JP \$+23 ;PATCHABLE BREAKPOINT
434D 00000000	2	481	DEFB 0,0,0,0,0,0,0,0,0
00000000			
0000			
4357 00000000	3	482	DEFB 0,0,0,0,0,0,0,0,0
00000000			
0000			
4361	391	485	OUTK 510+1,0300 ;CH-A RESET
4361 3E10	1	486	LD A,0300
4363 D361	2	487	OUT (510+1),A
4365	392	489	OUTK 510+3,0300 ;CH-B RESET
4365 3E10	1	490	LD A,0300
4367 D363	2	491	OUT (510+3),A
4369	393	493	OUTK 510+3,0020 ;PTR2 1CH-B1
4369 3E02	1	494	LD A,0020
436B D363	2	495	OUT (510+3),A
436D 212E40'	394	497	LD HL,S10VEC
4370 7D	395	498	LD A,L
4371 D363	396	499	OUT (510+3),A ;VECTOR TO WR2,PORT B
4373	397	500	OUTK 510+1,0240 ;RESET EXT,PTR4
4373 3E14	1	501	LD A,0240
4375 D361	2	502	OUT (510+1),A
4377	398	504	OUTK 510+1,01000100B ;X16,1STOF,NO PARITY -
4377 3E44	1	505	LD A,01000100B
4379 D361	2	506	OUT (510+1),A
437B	399	508	OUTK 510+1,0630 ;PTR3
437B 3E03	1	509	LD A,0630
437D D361	2	510	OUT (510+1),A
437F	400	512	OUTK 510+1,11000001B ;EBIT/CH,RX-ENBL
437F 3EE3	1	513	LD A,11000001B
4381 D361	2	514	OUT (510+1),A
4383	401	516	OUTK 510+1,0650 ;PTR5
4383 3E05	1	517	LD A,0650
4385 D361	2	518	OUT (510+1),A
4387	402	520	OUTK 510+1,11101010B ;DTR,RTS,EBIT/CH,TXENBL
4387 3EEA	1	521	LD A,11101010B

0094800

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43E7 D361      2 522      OUT (S10+1),A
43B8          403 524      OUTM S10+1,0210 ;P1SEL E1,P1R1
43E8 3E11      1 525      LD A,0210
43BD D361      2 526      OUT (S10+1),A
43BF          404 528      OUTM S10+1,00011010B ;INT ON ALL RX CHARS,--
43BF 3E1A      1 529      LD A,00011010B
4391 D361      2 530      OUT (S10+1),A
; --PARITY DOES NOT AFFECT VECTOR --
; --I1 INTERRUPT ENABLE,E1 DISABLE.
4393          407 534      OUTM S10+3,0010 ;P1R1 CH-B
4393 3E01      1 535      LD A,0010
4395 D363      2 536      OUT (S10+3),A
4397          408 538      OUTM S10+3,00000100B ;STATUS AFFECTS VECTOR CH
                        -B
4397 3E04      1 539      LD A,00000100B
4399 D363      2 540      OUT (S10+3),A
439B          409 542      BPT
439B C3B243    1 543      JP 4+23 ;PATCHABLE BREAKPOINT
439E 00000000  2 544      DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
43A8 00000000  3 545      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
; NOW LOAD MICRO-CODE FROM RAK 5000H TO SEQUENCER
43B2          411 548      BPT
43B2 C3C943    1 549      JP 4+23 ;PATCHABLE BREAKPOINT
43B5 00000000  2 550      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
43BF 00000000  3 551      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
43C9'210050   412 553 SBLDD LD HL,5000H
43CC 010000   413 554      LD BC,0
43CF'CDDE41'  414 555 1908 CALL SBLD
43D2 10FB     415 556      DJNZ 1908-B
43D4          416 557      BPT
43D4 C3EB43    1 558      JP 4+23 ;PATCHABLE BREAKPOINT
43D7 00000000  2 559      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
43E1 00000000  3 560      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
43EB 3EB0     417 562      LD A,0B0H
43ED D356     418 563      OUT (P102B),A ;ENBL SER & RESET
43EF          419 564      BPT
43EF C30644    1 565      JP 4+23 ;PATCHABLE BREAKPOINT
43F2 00000000  2 566      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
43FC 00000000  3 567      DEFB 0,0,0,0,0,0,0,0,0,0
00000000
0000
4406 3E30     420 569      LD A,30H
4408 D356     421 570      OUT (P102B),A ;ENBL CLOCK

```


442E E7	422 571	E6 A
443B 210000	423 572	LH HL,0
440F 110100	424 573	LD DE,I
4411'ED5A	425 574 11004	ADC HL,DE
4413 20FC	426 575	JR NZ,11004-8 ;SHORT DELAY FOR USED RESET
4415 3E2D	427 576	LD A,20H
4417 B356	428 577	DUI IP102B),A ;CLEAR RESET FLAG
4419	430 579	BPT
4419 C33044	1 580	JP #+23 ;PATCHABLE BREAKPOINT
441C 00000000	2 581	DEFB 0,0,0,0,0,0,0,0
00000000		
0000		
4426 00000000	3 582	DEFB 0,0,0,0,0,0,0,0
00000000		
0000		
4430 FB	431 584	EI
4431 DB54	432 585	IN A,(PI02) ;DUMMY READ TO SET RDY LINE
4433	433 586	BPT
4433 C34A44	1 587	JP #+23 ;PATCHABLE BREAKPOINT
4436 00000000	2 588	DEFB 0,0,0,0,0,0,0,0
00000000		
0000		
4440 00000000	3 589	DEFB 0,0,0,0,0,0,0,0
00000000		
0000		
444A C3004B'	434 591	JP BKSHND ; >>>>>>>>>>>>>>>>
		;***** ; INTERRUPT ROUTINES ; ;
444D'E5	438 595 ONESEC	PUSH HL
444E F5	439 596	PUSH AF
444F 214B41'	440 597	LD HL,CLOCK+3
4452 3E01	441 598	LD - A,I
4454 B6	442 599	ADD A,(HL)
4455 77	443 600	LD (HL),A
4456 3E00	444 601	LD A,0
445B 2B	445 602	DEC HL
4459 BE	446 603	ADC A,(HL)
445A 77	447 604	LD (HL),A
445B 3E00	448 605	LD A,0
445D 2B	449 606	DEC HL
445E BE	450 607	ADC A,(HL)
445F 77	451 608	LD (HL),A
4460 F1	452 609	PDP AF
4461 E1	453 610	POP HL
4462 FB	454 611	EI
4463 ED4D	455 612	RET ;INCREMENT RELATIVE SECONDS COUNTER
4465'F5	457 614 SIARCA	PUSH AF
4466 C5	458 615	PUSH BC
4467 E5	459 616	PUSH HL
4468	460 617	JNEV SIARCT
446B E5	1 618	PUSH HL
4469 CABB41'	2 619	LD HL,(SIARCT)
446F 23	3 620	JNC HL

0094800

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446E 3EE41' 4 621 LC (SIARC1),H
447E E1 5 622 FCF H
447J E6E44' 461 624 CALL STAST5 ;STATUS
447A 3A7241' 462 625 LD A,(HTJFL6) ;LOAD FLAG
4477 FE62 463 626 CP 2 ;IS IT 2? IE BUSY-F/G
4479 2007 464 627 JR N1,SIARC1-8 ;IF IT IS--
447B 465 628 TERM OE1H ;--- THEN ABORT. 00E100
447B 3EE1 1 629 LD A,OE1H
447D D350 2 630 OUT (PID),A
447F 76 3 631 HALT
4480 18FD 4 632 JR -1
4482 3E01 466 634 SIARC1 LD A,1
4484 327241' 467 635 LD (HTJFL6),A ;SET BUSY-F/G
4487 3A7341' 468 636 LD A,(HTJBCT) ;LOAD BYTE COUNT
448A 47 469 637 LD B,A ;SAVE
448B 217441' 470 638 LD HL,HTJTYT ;ADDR OF DATA START
448E B5 471 639 ADD A,L
448F 6F 472 640 LD L,A
449D 3E00 473 641 LD A,0
4492 8C 474 642 ADC A,H
4493 67 475 643 LD H,A ;HL NOW HAS NEW BYTE ADDRESS
4494 3AB641' 476 644 LD A,(SIATST)
4497 E601 477 645 AND 1
4499 2007 478 646 JR N2,SIARC3-8 ;OK IF CHAR AVAIL.
449B 479 647 TERM OE2H ;ABORT 00E200
449B 3EE2 1 648 LD A,OE2H
449D D350 2 649 OUT (PID),A
449F 76 3 650 HALT
44A0 18FD 4 651 JR -1
=44A2' 480 653 SIARC3 EQU 8
44A2 DB60 481 654 IN A,(SID) ;GET BYTE
44A4 77 482 655 LD (HL),A ;--AND STORE IT
44A5 DB61 483 656 IN A,(SID+1) ;RRO
44A7 E601 484 657 AND 1
44A9 2807 485 658 JR 2,SIARC4-8 ;OK IF NO MORE
44AB 486 659 TERM OE3H ;ABORT 00E300
44AB 3EE3 1 660 LD A,OE3H
44AD D350 2 661 OUT (PID),A
44AF 76 3 662 HALT
44B0 18FD 4 663 JR -1
=44B2' 487 665 SIARC4 EQU 8
44B2 78 488 666 LD A,B ;RECOVER COUNT
44B3 3C 489 667 INC A
44B4 327341' 490 668 LD (HTJBCT),A ;INCR & RESTORE
44B7 FE20 491 669 CP 32 ;IS IT 32
44B9 2005 492 670 JR N1,SIARC2-8 ;QUIT IF NOT --
44BB 3E02 493 671 LD A,2 ;--ELSE SET FLAG TO 2
44BD 327241' 494 672 LD (HTJFL6),A
44C0 E1 495 673 SIARC2 POP HL
44C1 C1 496 674 POP BC
44C2 F1 497 675 POP AF
44C3 FB 498 676 EI
44C4 ED4D 499 677 RETI

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; FOLLOWING IS A SUBROUTINE TO SIARC & SIARCA

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44C6 21B641' 502 680 SIATST LD HL,SIATST ;ADDR OF STATUS SAVE AREA
44C9 DB61 503 681 IN A,(SID+1) ;RRO

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0094800

44CB 77	504 682	LD (HL),A	;SAVE IT
44CC 23	505 683	INC HL	;NEXT
44CD	506 684	OUTX SID+1,0010	;PTR1
44CD 3E01	1 685	LD A,0010	
44CF D361	2 686	OUT (SID+1),A	
44D1 D861	507 688	IN A,(SID+1)	;RR1
44D3 77	508 689	LD (HL),A	;AND THIS ONE
44D4 E9	509 690	RET	
;			
44D5 CDC644	511 692 SIASRC	CALL SIASIS	;GET & SAVE STATUS
44D8	512 693	TERM OEOH	;ABORT SINCE THIS IS A SERIOUS ERROR 11E011
;			
44DB 3EE0	1 694	LD A,OEOH	
44DA D350	2 695	OUT (PID),A	
44DC 76	3 696	HALT	
44DD 1BFD	4 697	JR -1	
;			
44DF F5	514 700 SIATBE	PUSH AF	
44E0 C5	515 701	PUSH BC	
44E1 E5	516 702	PUSH HL	
44E2	517 703	INCV SIATCT	
44E2 E5	1 704	PUSH HL	
44E3 2AC041	2 705	LD HL,(SIATCT)	
44E6 23	3 706	INC HL	
44E7 22C041	4 707	LD (SIATCT),HL	
44EA E1	5 708	POP HL	
44EB 21B841	518 710	LD HL,SIADST	;OUT-STATUS AREA
44EE D861	519 711	IN A,(SID+1)	
44F0 77	520 712	LD (HL),A	
44F1 23	521 713	INC HL	
44F2	522 714	OUTX SID+1,0010	
44F2 3E01	1 715	LD A,0010	
44F4 D361	2 716	OUT (SID+1),A	
44F6 D861	523 718	IN A,(SID+1)	
44F8 77	524 719	LD (HL),A	;ABOVE SIMILAR TO SIDSTS
44F9 3AB841	525 720	LD A,(SIADST)	
44FC E604	526 721	AND 4	
44FE 2007	527 722	JR NZ,SIDTB3-4	;OK IF TBE
4500	528 723	TERM OD2H	;ABORT 11D211
4500 3ED2	1 724	LD A,OD2H	
4502 D350	2 725	OUT (PID),A	
4504 76	3 726	HALT	
4505 1BFD	4 727	JR -1	
=4507	529 729 SIDTB3	EDU 1	
4507 3A9441	530 730	LD A,(INTDFLG)	
450A FE02	531 731	CP 2	;COMP FLAG WITH 2
450C 2B07	532 732	JR Z,SIDTB1-4	;OK IF 2
450E	533 733	TERM OD1H	;ELSE ABORT
450E 3ED1	1 734	LD A,OD1H	
4510 D350	2 735	OUT (PID),A	
4512 76	3 736	HALT	
4513 1BFD	4 737	JR -1	
4515 3A9541	534 739 SIDTB1	LD A,(HTOECT)	
4518 47	535 740	LD E,A	
4519 219641	536 741	LD HL,HICSER	
451C B5	537 742	ADD A,L	
451D 8F	538 743	LD L,A	

0094800

4520 0000	548 748	LD A,0	
4521 00	549 749	ADC A,A	
4522 07	549 749	LD H,F	
4523 7E	542 747	LD A,(HL)	;ABOVE SAME AS RECEIVED CODE
4523 1360	543 748	OUT (SIO),A	;OUTPUT NEXT CHAR
4525 7E	544 749	LD A,S	
4526 3C	545 750	INC A	
4527 FE20	546 751	CP 32	;IS NEW COUNT 32
4529 2004	547 752	JR -S10TB2-8	;IF NOT--NORMAL RETURN
452B AF	548 753	XOR A	;OTHERWISE ZERO COUNT AND FLAG

6

452C 329441'	549 754	LD (HIOFL6),A	
452F'329541'	550 755 S10TB2	LD (HIOBCT),A	
4532 E1	551 756	PDP HL	
4533 C1	552 757	PDP BC	
4534 F1	553 758	PDP AF	
4535 FB	554 759	E1	
4536 ED4D	555 760	RETJ	

4538'F5	557 762 P1A1K	PUSH AF	
4539 C5	558 763	PUSH BC	
453A E5	559 764	PUSH HL	
453B	560 765	INCM P1A1CT	
453B E5	1 766	PUSH HL	
453C 2AC241'	2 767	LD HL,(P1A1CT)	
453F 23	3 768	INC HL	
4540 22C241'	4 769	LD (P1A1CT),HL	
4543 E1	5 770	PDP HL	
4544 3A6541'	561 772	LD A,(H51FL6)	;AS FOR SIARCA
4547 FE02	562 773	CP 2	
4549 2007	563 774	JR N1,P1A1K1-8	
454B	564 775	TERM OC1H	;ABORT 88C188
454B 3EC1	1 776	LD A,OC1H	
454D B350	2 777	OUT (P1D),A	
454F 76	3 778	HALT	
4550 1BFD	4 779	JR -1	
4552'3E01	565 781 P1A1K1	LD A,1	
4554 32A541'	566 782	LD (H51FL6),A	;SET BUSY F/6
4557 3A6641'	567 783	LD A,(H51BCT)	
455A 47	568 784	LD B,A	
455B 216741'	569 785	LD HL,H51SCH	
455E 85	570 786	ADD A,L	
455F 6F	571 787	LD L,A	
4560 3E00	572 788	LD A,0	
4562 8C	573 789	ADC A,H	
4563 67	574 790	LD H,A	
4564 DB54	575 791	IN A,(P1D2)	
4566 77	576 792	LD (HL),A	
4567 7B	577 793	LD A,B	
456B 3C	578 794	INC A	
4569 326641'	579 795	LD (H51BCT),A	
456E FE09	580 796	CP 9	;ONLY 9 BYTES IN BLOCK
456E 2005	581 797	JR N1,P1A1K2-8	
4570 3E02	582 798	LD A,2	
4572 326541'	583 799	LD (H51FL6),A	
4575'E1	584 800 P1A1K2	PDP HL	
4576 C1	585 801	PDP BC	

RAD ORIGINAL

0094800

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4577 F1      5E6 E02      1E3 AF
457E F1      5E7 E03      E1
4579 E14D    5E8 B04      RETI

457B F5      590 B01 PIAOU1 PUSH AF
457C 3AC441' 591 B07      LD A,(PIAUCT)
457F B7      592 B08      DR A
4580 200D    593 B09      JR N1,PIADU2-8
4582 3AC541' 594 B10      LD A,(PIAUCT+1)
4585 B7      595 B11      DR A
4586 2007    596 B12      JR N1,PIADU2-8
458B 3E01    597 B13      LD A,1
458A 32C441' 598 B14      LD (PIAUCT),A
458D 1817    599 B15      JR PIAOU1-8
458F'        600 B16 PIAOU2 JNCV PIAUCT
458F E5      1 B17      PUSH HL
4590 2AC441' 2 B18      LD HL,(PIAUCT)
4593 23      3 B19      JNC HL
4594 22C441' 4 B20      LD (PIAUCT),HL
4597 E1      5 B21      POP HL
4598 3A7041' 601 B23      LD A,(KSOFL6)
459B FE02    602 B24      CP 2
459D 2B07    603 B25      JR 2,PIADU1-8 ;DK IF 2
459F'        604 B26      TERK OB1H ;ABORT 11B111
459F 3EB1    1 B27      LD - A,OB1H
45A1 D350    2 B28      OUT (PID),A
45A3 76      3 B29      HALT
45A4 1BFB    4 B30      JR -1
45A6 AF'     605 B32 PIAOU1 XOR A
45A7 327041' 606 B33      LD (KSOFL6),A ;SET FREE
45AA F1      607 B34      POP AF
45AB FB      608 B35      EI
45AC ED4D    609 B36      RETI

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;
;
;
4800          612 B39      ORS 4800H ;NEXT RDK
=4800'        613 B40 BCKEND EQU 4 ;BACKGROUND LOOP
4800          614 B41      BPT
4800 E3174B   1 B42      JP 4+23 ;PATCHABLE BREAKPOINT
4803 00000000 2 B43      DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
480D 00000000 3 B44      DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
4817 3A6541' 615 B46      LD A,(KSI1F6)
481A FE02    616 B47      CP 2
481C E2314B' 617 B48      JP W2,BCX046 ;BYPASS NSIO IF NOT 2
481F'        618 B49      JNCV XREADS
481F E3      1 B50      PUSH HL
4820 2A5141' 2 B51      LD HL,(XREADS)
4823 23      3 B52      INC HL
4824 225141' 4 B53      LD (XREADS),HL
4827 E1      5 B54      POP HL
482B'        619 B56      FILL PARWK,PARWK+PARWK1-1,0 ;CLEAR WORKAREA
482B 3E00    4 B60      LD A,0
482A 11E641' 5 B61      LD DE,PARWK

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BAD ORIGINAL

0094800

4E30 12	6 E27	LD H,H	
4E31 20	7 E28	LD H,H	
4E32 2F	8 E29	LD L,E	
4E33 13	9 E2A	INC DE	
4E34 010760	10 E2B	LD BC,RES.PARITY+PARNKL-1-PARITY	
4E35 E260	11 B67	LDIR	
4E36 3A6F41	620 B69	LD A,(MSDATA+7) ;PARITY BYTE	
4E39 DD7703	621 B70	LD (11+3),A ;SAVE	
4E3C 4F	622 B71	LD C,A ;AND IN C	
4E3D E603	623 B72	AND 3	
4E3F EA4648	624 B73	JP PE,BCK002	
4E42 DDCB00C6	625 B74	SET 0,(11)	
4E46 79	626 B75 BCK002	LD A,C	
4E47 E60C	627 B76	AND 0CH	
4E49 EA504B	628 B77	JP PE,BCK003	
4E4C DDCB00CE	629 B78	SET 1,(11)	
4E50 79	630 B79 BCK003	LD A,C	
4E51 E630	631 B80	AND 30H	
4E53 EA5A4B	632 B81	JP PE,BCK004	
4E56 DDCB00D6	633 B82	SET 2,(11)	
4E5A 79	634 B83 BCK004	LD A,C	
4E5B E6C0	635 B84	AND 0C0H	
4E5D EA644B	636 B85	JP PE,BCK005	
4E60 DDCB00DE	637 B86	SET 3,(11)	
=4E64	638 B87 BCK005	EDU 4	
			;FIRST WORD SET TO INDICATE A
			GREEMENT
			; BETWEEN PARITY BIT PAIRS.
4E64 3A6E41	640 B89	LD A,(MSDATA+6) ;ECC BYTE	
4E67 F5	641 B90	PUSH AF	
4E6B E63F	642 B91	AND 3FH	;LEAVE 5-0 ONLY
4E6A DD7704	643 B92	LD (11+4),A	;SAVE IN WORKAREA
4E6D F1	644 B93	POP AF	
4E6E 07	645 B94	RLCA	
4E6F 07	646 B95	RLCA	
4E70 57	647 B96	LD D,A	;ECC 6 BITS LEFT ADJ.
4E71 E603	648 B97	AND 3	
4E73 6F	649 B98	LD L,A	;SAVE MOD 4
4E74 7A	650 B99	LD A,D	
4E75 1600	651 900	LD D,0	
4E77 0606	652 901	LD B,6	
4E79 B7	653 902 BCK006	OR A	
4E7A F27E4B	654 903	JP P,BCK007	
4E7D 14	655 904	INC D	
4E7E 07	656 905 BCK007	RLCA	
4E7F 10FB	657 906	DJNZ BCK006-4	
4E81 7A	658 907	LD A,D	;D HAS NO OF 1'S IN ECC 5-0
4E82 E603	659 908	AND 3	
4E84 95	660 909	SUB 1	
4E85 2B04	661 910	JR 2,BCK008-8	
4E87 DDCB00FE	662 911	SET 7,(11)	;SET IF ERROR IN MOD 4
4E8B 3A6D41	663 912 BCK008	LD A,(MSDATA+5) ;LSBYTE	
4E8E 0E00	664 913	LD C,0	
4E90 B7	665 914	OR A	
4E91 E29B4B	666 915	JP PD,BCK009	
4E94 3E03	667 916	LD A,3	
4E96 B1	668 917	OR C	
4E97 4F	669 918	LD C,A	

BAD ORIGINAL

0094800

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4E5E'3F541'  676 919 E21009 LD  A,(MSDATA+4)
4E5E E7       671 920 GE  A
4E5E E2A34E'  672 921 JP  PD,BCK010
4E5F 2E6C     673 922 LD  A,0CH
4E61 B1       674 923 OR  C
4E62 4F       675 924 LD  C,A
4E63'3A6B41'  676 925 BCK010 LD  A,(MSDATA+3)
4E66 B7       677 926 OR  A
4E67 E2A64B'  678 927 JP  PD,BCK011
4E6A 3E30     679 928 LD  A,30H
4E6C B1       680 929 OR  C
4E6D 4F       681 930 LD  C,A
4E6E'3A6A41'  682 931 BCK011 LD  A,(MSDATA+2)
4E61 B7       683 932 OR  A
4E62 E2B94B'  684 933 JP  PD,BCK012
4E65 3E60     685 934 LD  A,0COH
4E67 B1       686 935 OR  C
4E68 4F       687 936 LD  C,A
4E69'79       688 937 BCK012 LD  A,C
4E6A DDAE03   689 938 XOR  (IX+3) ;ACTUAL PARITY BYTE
4E6D DD7701   690 939 LD  (IX+1),A ;1'S FOR PARITY FAILURE

;
4E6C 216A41'  692 941 LD  HL,MSDATA+2 ;MSBYTE
4E63 C67E     693 942 BIT  7,(HL) ;BIT 31 OF DATA
4E65 2004     694 943 JR   NZ,BCK013-8
4E67 DDCB02EE 695 944 SET  5,(IX+2) ;ECC BIT 5
4E6B'0605     696 945 BCK013 LD  B,5
4E6D 0E00     697 946 LD  C,0
4E6F 215940'  698 947 LD  HL,MASK0
4E67'CD3142'  699 948 BCK015 CALL ECC ;CHECKS ONE BIT RETURNED IN A
;                                     CC
;                                     ; HL INCR BY 4

4E65 B7       701 950 OR  A
4E66 2810     702 951 JR   Z,BCK014-8
4E68 79       703 952 LD  A,C
4E69 CB27     704 953 SLA  A
4E6B CB27     705 954 SLA  A
4E6D CB27     706 955 SLA  A
4E6F F6C6     707 956 OR  0C6H
4E61 32E74B'  708 957 LD  (SETB+3),A ;OVERLAY INSTR WITH BIT NO
4E64'DDCB02C6 709 958 SETB SET  0,(IX+2)
4E6B'0C       710 959 BCK014 INC  C ;NEXT BIT
4E69 10E7     711 960 DJNZ BCK015-8 ;DO IT AGAIN
; ECC 5-0 NOW CALCULATED IN (IX+2)

4E6B DD7E02   713 962 LD  A,(IX+2)
4E6E DDAE04   714 963 XOR  (IX+4) ;ACTUAL ECC 5-0
4E61 DD7702   715 964 LD  (IX+2),A ;STORE 1'S FOR ECC FAILURE
4E64 DDB601   716 965 OR  (IX+1) ;OR IN PARITY FAILURES
4E67 DDB600   717 966 OR  (IX) -- ;OR IN PARITY PAIR FAILS AND
;                                     MOD 4

4E6A CA7A49'  718 967 JP   Z,BCK016 ;JUMP ON TOTALLY GOOD BLOCK
4E6D         719 968 INCW NPE1N1 ;INITIAL PHYSER COUNTER
4E6D E5       1 969 PUSH HL
4E6E 2A5541'  2 970 LD  HL,(NPE1N1)
4901 23       3 971 INC  HL
4902 225541'  4 972 LD  (NPE1N1),HL
4905 E1       5 973 POP  HL

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0094800

4906 1E7E00	720 975	LD A, (11)	
4908 E7	721 976	ER A	
490A 12BA49'	722 977	JP NZ, ECI017	; UNCORRECTABLE ERROR ; -DUE TO MSD4 OR ECC OR PARITY PAIR ERROR
490D DD7E01	724 979	LD A, (11+1)	; PARITY FAILS
4910 0E00	725 980	LD C, 0	
4912 0608	726 981	LD B, 8	
4914' EB07	727 982 PCK019	RLC A	
4916 F21A49'	728 983	JP P, BCK018	
4919 0C	729 984	JNC C	
491A' 10F8	730 985 BCK018	DJNZ BCK019-1	
491C 79	731 986	LD A, C	
491D EB3F	732 987	SRL A	; NO OF PARITY FAILS
491F DD7707	733 988	LD (11+7), A	
4922 FE01	734 989	CP 1	
4924 C2BA49'	735 990	JP NZ, BCK017	; UNCORR IF 1 PARERRS NOT 1
4927 DD7E02	736 991	LD A, (11+2)	
492A B7	737 992	DR A	
492B CABA49'	738 993	JP Z, BCK017	; UNCORR UNLESS ECC FAIL
492E 3D	739 994	DEC A	
492F DD7705	740 995	LD (11+5), A	; FAILED BIT NO
4932 4F	741 996	LD C, A	
4933 EB3F	742 997	SRL A	
4935 EB3F	743 998	SRL A	
4937 EB3F	744 999	SRL A	; A HAS FAILED BYTE 0-LSBYT, 3-MSBYT
4939 DD7706	745 1000	LD (11+6), A	
493C 79	746 1001	LD A, C	
493D CB27	747 1002	SLA A	
493F E630	748 1003	AND 30H	
4941 4F	749 1004	LD C, A	
4942 3E46	750 1005	LD A, 46H	
4944 B1	751 1006	DR C	
4945 324B49'	752 1007	LD (FBIT+3), A	; OVERLAY BIT INSTR
494B' DDCB0146	753 1008 FBIT	BIT 0, (11+1)	; THIS SHOULD BE 1
494E CABA49'	754 1009	JP Z, BCK017	; IF 0 ECC AND PARITY DONT AGR EE
494F DD5E06	755 1010	LD E, (11+6)	; BYTE NO
4952 1600	756 1011	LD B, 0	
4954 216D41'	757 1012	LD HL, MSDATA+5	
4957 B7	758 1013	DR A	
4958 ED52	759 1014	SBC HL, DE	; HL<-ACTUAL DUD BYTE ADDRESS
495A DD7E05	760 1015	LD A, (11+5)	
495D E607	761 1016	AND 7	
495F CB27	762 1017	SLA A	
4961 CB27	763 1018	SLA A	
4963 CB27	764 1019	SLA A	
4965 F6E0	765 1020	DR 0E0H	
4967 0600	766 1021	LD B, 0	
4969 326049'	767 1022	LD (SETIN+1), A	; OVERLAY INST
496C' CBC0	768 1023 SETIN	SET 0, B	
496E 7E	769 1024	LD A, (HL)	
496F A8	770 1025	JOR B	
4970 77	771 1026	LD (HL), A	; INVERT DUD BIT
4971	772 1027	INCW NPERCO	; CORRECTION COUNTER
4971 E5	1 1028	PUSH HL	

BAD ORIGINAL


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4972 2A5741' 2 1029 LD HL, (PC+1)
4975 23 3 1030 INC HL
4976 225741' 4 1031 LD (PC+2), HL
4979 E1 5 1032 POP HL

;
=497A' 774 1035 BCK016 EQU 0 ; TO HERE IF GOOD OR CORRECTED
497A 3AEB41' 775 1036 LD A, (MSDATA)
497D E60F 776 1037 AND 15 ; RESIDUAL TIME
497F 2032 777 1038 JR NZ, BCK020 ; TO LOGICAL TESTS IF NOT TIME
; OUT
4981 77B 1039 INCW NPERTO ; INC PHYSERRS DUE TO TIME-OUT
T

4981 E5 1 1040 PUSH HL
4982 2A5341' 2 1041 LD HL, (NPERTO)
4985 23 3 1042 INC HL
4986 225341' 4 1043 LD (NPERTO), HL
4989 E1 5 1044 POP HL

;
=498A' 780 1047 BCK017 EQU 0 ; TO HERE IF ULTIMATELY A PHYS
ERR.

498A 781 1048 BPT
498A C3A149 1 1049 JP 9+23 ; PATCHABLE BREAKPOINT
498D 00000000 2 1050 DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
4997 00000000 3 1051 DEFB 0,0,0,0,0,0,0,0,0
00000000
0000

49A1 782 1053 INCW NPHYER
49A1 E5 1 1054 PUSH HL
49A2 2A5B41' 2 1055 LD HL, (NPHYER)
49A5 23 3 1056 INC HL
49A6 225B41' 4 1057 LD (NPHYER), HL
49A9 E1 5 1058 POP HL
49AA 3E01 783 1060 LD A, 1
49AC 324441' 784 1061 LD (ACKCD), A
49AF F3 785 1062 DI
49B0 C3F94A' 786 1063 JP BCK047 ; TO MSOUTPUT SECTION

;
=49B3' 788 1065 BCK020 EQU 0 ; LOGICAL TESTS
49B3 789 1066 BPT
49B3 C3CA49 1 1067 JP 9+23 ; PATCHABLE BREAKPOINT
49B6 00000000 2 1068 DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
49C0 00000000 3 1069 DEFB 0,0,0,0,0,0,0,0,0
00000000
0000

49CA 3A6441' 790 1071 LD A, (MSDATA+21) ; MSBYTE
49CD 4F 791 1072 LD C, A
49CE 07 792 1073 RLCA
49CF 07 793 1074 RLCA
49D0 E603 794 1075 AND 3 ; TYPE IN ACC
49D2 2006 795 1076 JR NZ, BCK021-4 ; SKIP IF NOT LOG
49D4 EB49 796 1077 B11 5, C
49D6 2B02 797 1078 JR Z, BCK021-4 ; SKIP IF BIT 29=0
49D8 3E04 798 1079 LD A, 4

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496A'324041'	799 1080	BEK021	LD	(TYPE),A	
49DD 3A6741'	800 1081		LD	A,(INSECH)	
49ED 1F	801 1082		RRA		
49E1 E67F	802 1083		AND	7FH	;S/C NO
49E3 324341'	803 1084		LD	(SUBCHA),A	
49E6 5F	804 1085		LD	E,A	
49E7 1600	805 1086		LD	D,0	
49E9 21005B	806 1087		LD	HL,SUBCHS	;SUE-CHAN STATUS AREA
49EC EB	807 1088		EX	DE,HL	
49ED 29	808 1089		ADD	HL,HL	
49EE 29	809 1090		ADD	HL,HL	
49EF 29	810 1091		ADD	HL,HL	
49FO 29	811 1092		ADD	HL,HL	;MULT S/C BY 16
49F1 B7	812 1093		OR	A	
49F2 ED5A	813 1094		ADC	HL,DE	;HL←ADDRESS OF S/C SLOT
49F4 ES	814 1095		PUSH	HL	
49F5 FDE1	815 1096		PDP	IY	
49F7 7E	816 1097		LD	A,(HL)	;STATE
49FB 324141'	817 1098		LD	(CSTATE),A	
49FB 4F	818 1099		LD	C,A	
49FC 3A4041'	819 1100		LD	A,(TYPE)	
49FF CB27	820 1101		SLA	A	
4A01 CB27	821 1102		SLA	A	
4A03 81	822 1103		ADD	A,C	
4A04 5F	823 1104		LD	E,A	
4A05 1600	824 1105		LD	D,0	
4A07 B7	825 1106		OR	A	
4A08 214540'	826 1107		LD	HL,STABLE	
4A0B ED5A	827 1108		ADC	HL,DE	
4A0D 7E	828 1109		LD	A,(HL)	;TRANSITION TABLE CELL
4A0E 324241'	829 1110		LD	(CELL),A	
4A11 3A4141'	831 1112		LD	A,(CSTATE)	
4A14 B7	832 1113		OR	A	
4A15 2B34	833 1114		JR	Z,BCK022-8	
4A17 3A4041'	834 1115		LD	A,(TYPE)	
4A1A B7	835 1116		OR	A	
4A1B 202E	836 1117		JR	NZ,BCK022-8	
4A1D 3A6D41'	837 1118		LD	A,(MSDATA+5)	
4A20 FDBE05	838 1119		CP	(IY+5)	
4A23 201E	839 1120		JR	NZ,BCK023-8	
4A25 3A6C41'	840 1121		LD	A,(MSDATA+4)	
4A28 FDBE04	841 1122		CP	(IY+4)	
4A2B 2016	842 1123		JR	NZ,BCK023-8	
4A2D 3A6B41'	843 1124		LD	A,(MSDATA+3)	
4A30 FDBE03	844 1125		CP	(IY+3)	
4A33 200E	845 1126		JR	NZ,BCK023-8	
4A35 3A6A41'	846 1127		LD	A,(MSDATA+2)	
4A38 E61F	847 1128		AND	1FH	
4A3A 4F	848 1129		LD	C,A	
4A3B FD7E02	849 1130		LD	A,(IY+2)	
4A3E E61F	850 1131		AND	1FH	
4A40 B9	851 1132		CP	C	
4A41 280B	852 1133		JR	Z,BCK022-8	
4A43 3A4241'	853 1134	BEK023	LD	A,(CELL)	
4A46 F630	854 1135		OR	.30H	;ON BITS 5,4 IE LOG ERROR

--DUE TO LOG CARD OF DIFF. OPERATOR TRYING.

0094800

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; --TO LOGON WHEN STATEMENT ELSE IS ON.
4A4B 324241' 857 1138 LD (CELL),A
;
;=4A4B' 859 1140 BCK022 EQU 0 ;NOW BUILD TRANSACTION ENTRY
; IN TABLE
4A4B 860 1141 BPT
4A4B C3624A 1 1142 JP 8+23 ;PATCHABLE BREAKPOINT
4A4E 00000000 2 1143 DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
4A5B 00000000 3 1144 DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
4A62 3A4341' 861 1146 LD A,(SUBCHA)
4A65 110060 862 1147 LD DE,TRANST
4A68 2A1B41' 863 1148 LD HL,(LSTRND)
4A6B 29 864 1149 ADD HL,HL
4A6C 29 865 1150 ADD HL,HL
4A6D 29 866 1151 ADD HL,HL ;MULT BY 8
4A6E B7 867 1152 DR A
4A6F ED5A 868 1153 ADC HL,DE
; HL NOW HAS ADDRESS OF TRANS SLOT
4A71 77 870 1155 LD (HL),A
4A72 23 871 1156 INC HL
4A73 E5 872 1157 PUSH HL
4A74 F3 873 1158 DI
4A75 3A4641' 874 1159 LD A,(CLOCK+1)
4A7B EA03 875 1160 AND 3
4A7A 77 876 1161 LD (HL),A
4A7B 23 877 1162 INC HL
4A7C 3A4741' 878 1163 LD A,(CLOCK+2)
4A7F 77 879 1164 LD (HL),A
4A80 23 880 1165 INC HL
4A81 3A4841' 881 1166 LD A,(CLOCK+3)
4A84 77 882 1167 LD (HL),A
4A85 FB 883 1168 EI
4A86 23 884 1169 INC HL
4A87 EB 885 1170 EI DE,HL
4A8B 216A41' 886 1171 LD HL,MSDATA+2
4A8B 010400 887 1172 LD BC,A
4A8E EDB0 888 1173 LDIR
4A90 E1 889 1174 POP HL ;BYTE 2 ADDR OF SLOT
4A91 3A4241' 890 1175 LD A,(CELL)
4A94 E6F0 891 1176 AND OF0H
4A96 B6 892 1177 DR (HL)
4A97 77 893 1178 LD (HL),A ;PREV STATE & ERR BITS
;
4A9B 3A4241' 895 1180 LD A,(CELL)
4A9B 07 896 1181 RLCA
4A9C 07 897 1182 RLCA
4A9D 07 898 1183 RLCA
4A9E 07 899 1184 RLCA
4A9F E602 900 1185 AND 2 ;BIT 5 OF CELL TO A(1)
;
4AA1 324441' 902 1187 LD (ACKED),A
4AA1 F3 903 1188 DI
4AA5 B7 904 1189 DR A

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4AAB 203E      905 1190      JR  N7,BCK024 ;IF LOG ERR
4AAB          906 1191      INCW N6000
4AAB E5        1 1192      PUSH HL
4AA9 2A5941'   2 1193      LD  HL,(N6000)
4AAC 23        3 1194      INC  HL
4AAD 225941'   4 1195      LD  (N6000),HL
4AE0 E1        5 1196      POP  HL
4AB1 3A4741'   907 1198      LD  A,(CELL)
4AB4 E603      908 1199      AND  3 ;NEW STATE
4AB6 FD7700    909 1200      LD  (1Y),A ;10 SLOT IN S/C TABLE
4AB9 FE00      910 1201      CP   0
4ABB 200E      911 1202      JR  N7,DH44B-8
4ABD FD7702    912 1203      LD  (1Y+2),A
4AC0 FD7703    913 1204      LD  (1Y+3),A
4AC3 FD7704    914 1205      LD  (1Y+4),A
4AC6 FD7705    915 1206      LD  (1Y+5),A ;ZERO OPERATOR ID IF NEW STAT
                                     E 0
4AC9 1B1C      916 1207      JR  BCK025-8
4ACB'FE01      917 1208 DH44B CP   1
4ACD 2018      918 1209      JR  N7,BCK025-8
                                     ;HERE IF NEWSTATE 1 AND GOOD TRANS
4ACF 216A41'   920 1211      LD  HL,MSDATA+2
4AD2 FDES      921 1212      PUSH 1Y
4AD4 D1        922 1213      POP  DE
4AD5 13        923 1214      INC  DE
4AD6 13        924 1215      INC  DE
4AD7 010400    925 1216      LD  BC,4
4ADA EDB0      926 1217      LD1R ;COPY NEW OPERATOR CODE TO S/
                                     C SLOT
4ADC 1B09      927 1218      JR  BCK025-8
4ADE'          928 1219 BCK024 INCW NLOGER
4ADE E5        1 1220      PUSH HL
4ADF 2A5D41'   2 1221      LD  HL,(NLOGER)
4AE2 23        3 1222      INC  HL
4AE3 225D41'   4 1223      LD  (NLOGER),HL
4AE6 E1        5 1224      POP  HL
4AE7'          929 1226 BCK025 INCW LSTRND
4AE7 E5        1 1227      PUSH HL
4AEB 2A4B41'   2 1228      LD  HL,(LSTRND)
4AEB 23        3 1229      INC  HL
4AEC 224B41'   4 1230      LD  (LSTRND),HL
4AEF E1        5 1231      POP  HL
4AF0          930 1233      DECW NLEFT
4AF0 E5        1 1234      PUSH HL
4AF1 2A4D41'   2 1235      LD  HL,(NLEFT)
4AF4 2B        3 1236      DEC  HL
4AF5 224D41'   4 1237      LD  (NLEFT),HL
4AF8 E1        5 1238      POP  HL
4AF9'          931 1240 BCK047 BPI
4AF9 C3104B    1 1241      JP  8+23 ;PATCHABLE BREAKPOINT
4AFC 00000000   2 1242      DEFB 0,0,0,0,0,0,0,0,0
      00000000
      0000
4B0B 00000000   3 1243      DEFB 0,0,0,0,0,0,0,0,0
      00000000
      0000
4B10 3A2041'   932 1245      LD  A,(NSOFL6)

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4B13 B7      533 1246      DR  A
4B14 2B02     534 1247      JR  1,BE102E-1
4B16 1B1B     935 1248      JR  V645-1
4B1B*3E02     936 1249 BCK026 LD  A,2
4B1A 327041'  937 1250      LD  (MSOFL6),A ;SET F/6 BUSY
4B1D 3A4441'  938 1251      LD  A,(ACKED)
4B20 D354     939 1252      OUT (F102),A ;ACK CODE
4B22          940 1253      FILL MSIFL6,MSDATA+7,0
4B22 3E00      4 1257      LD  A,0
4B24 116541'  5 1258      LD  DE,MSIFL6
4B27 12        6 1259      LD  (DE),A
4B28 62        7 1260      LD  H,D
4B29 6B        8 1261      LD  L,E
4B2A 13        9 1262      INC  DE
4B2B 010A00    10 1263     LD  BC,.RES.MSDATA+7-MSIFL6
4B2E EDB0      11 1264     LDTR
4B30*FB        941 1266 V645  EI

;
4B31'          943 1268 BCK046 BPT
4B31 C34B4B     1 1269      JP  1+23 ;PATCHABLE BREAKPOINT
4B34 00000000   2 1270      DEFB 0,0,0,0,0,0,0,0,0,0
      00000000
      0000
4B3E 00000000   3 1271      DEFB 0,0,0,0,0,0,0,0,0,0
      00000000
      0000
4B4B 3A7241'   944 1273      LD  A,(HTIFL6)
4B4B FE02       945 1274      CP  2
4B4D C2644D'   946 1275      JP  N7,BCK027 ;BYPASS HOST INPUT
4B50 217441'   947 1276      LD  HL,HTITVP
4B53 CD0042'   948 1277      CALL CHKSUM
4B56 21BA41'   949 1278      LD  HL,INCK1
4B59 119041'   950 1279      LD  DE,HTICK1
4B5C 0604      951 1280      LD  B,4
4B5E*1A        952 1281 BCK028 LD  A,(DE)
4B5F BE        953 1282      CP  (HL)
4B60 2006      954 1283      JR  N7,BCK029-1
4B62 23        955 1284      INC  HL
4B63 13        956 1285      INC  DE
4B64 10FB      957 1286      DJNZ BCK028-1
4B66 1B72      958 1287      JR  BCK030-1 ;CHECKSUMS ARE EQUAL

;
      =4B6B* 960 1289 BCK029 EDU 1 ;NOT EQUAL
4B6B 3E22      961 1290      LD  A,34 ;ERROR CODE = DUD CHASUM AND
      RETRANSMIT

;
4B6A'          963 1292 HTOFMT BPT
4B6A C3B14B     1 1293      JP  1+23 ;PATCHABLE BREAKPOINT
4B6D 00000000   2 1294      DEFB 0,0,0,0,0,0,0,0,0,0
      00000000
      0000
4B77 00000000   3 1295      DEFB 0,0,0,0,0,0,0,0,0,0
      00000000
      0000
4B81 32AD41'   964 1297      LD  (HTOERC+1),A
4B84 CD5E42'   965 1298      CALL HTDF ;BUILD DEFAULT MESSAGE
4B87 CD4C42'   966 1299      CALL HTDCSH

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4E8A	967 1300	INCK MSHIN
4E8A ES	1 1301	PUSH HL
4E8E 2A6141'	2 1302	LD HL, (MESHIN)
4E8E 23	3 1303	INC HL
4E8F 226141'	4 1304	LD (MESHIN), HL
4B92 E1	5 1305	PDP HL
4B93'	96B 1307 SEND	BPT
4E93 C3A44B	1 1308	JP 9423 ;PATCHABLE BREAKPOINT
4B96 00000000	2 1309	DEFB 0,0,0,0,0,0,0,0,0
00000000		
0000		
4BA0 00000000	3 1310	DEFB 0,0,0,0,0,0,0,0,0
00000000		
0000		
4BAA 3A9441'	969 1312	LD A, (HIDFL6)
4BAD B7	970 1313	DR A
4BAE 2807	971 1314	JR 2, BCK031-8
4BB0	972 1315	TERM 21H ;ABORT 882188
4BB0 3E21	1 1316	LD A, 21H
4BB2 D350	2 1317	OUT (PIO), A
4BB4 76	3 1318	HALT
4BB5 18FD	4 1319	JR -1
4BB7'F3	973 1321 BCK031	DI
4BB8 3E01	974 1322	LD A, 1
4BBA 329541'	975 1323	LD (HTOBC1), A
4BBD 3C	976 1324	INC A
4BBE 329441'	977 1325	LD (HTOFL6), A
4BC1 3A9441'	978 1326	LD A, (HTOSER)
4BC4 D360	979 1327	OUT (SID), A ;FIRST CHARACTER
4BC6 AF	980 1328	XOR A
4BC7 327341'	981 1329	LD (HTIBCT), A
4BCA 327241'	982 1330	LD (HTJFL6), A
4BCD FB	983 1331	E1
4BCE	984 1332	INCK MHDUT
4BCE ES	1 1333	PUSH HL
4BCF 2A6341'	2 1334	LD HL, (MHDUT)
4BD2 23	3 1335	INC HL
4BD3 226341'	4 1336	LD (MHDUT), HL
4BD6 E1	5 1337	PDP HL
4BD7 C3644D'	985 1339	JP BCK027
=4BDA'	987 1341 BCK030	EQU 8 ;BUILD REAL DUT MESSAGE
4BDA 3A7441'	988 1342	LD A, (HT11YP)
4BDD FEFF	989 1343	CP -1
4BDF 2027	990 1344	JR N7, BCK032-8 ;JP IF NOT FULL RESET
4BE1 246041'	991 1345	LD HL, (HT11YP*12)
4BE4 110B03	992 1346	LD DE, 030BH
4BE7 B7	993 1347	OR A
4BED EDS2	994 1348	SEC HL, DE
4BEA 2017	995 1349	JR -N7, BCK033-8 ;DUD
4BEC 2A8B41'	996 1350	LD HL, (HT11YP*20)
4BEF 1100B9	997 1351	LD DE, 69D0H
4BF2 B7	998 1352	OR A
4BF3 EDS2	999 1353	SEC HL, DE
4BF5 200C	1000 1354	JR N7, BCK033-8 ;DUD
4BF7 2A8C41'	1001 1355	LD HL, (HT11YP*24)
4BFA 110434	1002 1356	LD DE, 3404H

0094800

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45FD B7      1003 1357      OR  A
4BFE ED52    1004 1358      SBC  HL,DE
4C00 CA0000  1005 1359      JP   Z,0      ;OK-COMplete RESET !! >>>>>>
                                     >>>

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4C03'3EB2    1007 1361 BCK033 LD  A,130      ;DUD CONST AND RESEND
4C05 C36A4B' 1008 1362      JP   HTDFMT

;
4C0B'F101    1010 1364 BCK032 CP   J
4C0A CA174C' 1011 1365      JP   2,BCK034      ;DID RESET
4C0D FE00    1012 1366      CP   0
4C0F CAB74C' 1013 1367      JP   2,BCK035      ;TRANS REQUEST
4C12 3E42    1014 1368      LD   A,66      ;INV TRANS TYPE AND RESEND
4C14 C36A4B' 1015 1369      JP   HTDFMT
4C17'3A7741' 1016 1370 BCK034 LD  A,(HT1PRT+1) ;DID S/C TO RESET
4C1A B7      1017 1371      OR   A
4C1B FA0A00  1018 1372      JP   1,BCK037-8 ;ERROR IF >127
4C1E 4F      1019 1373      LD   C,A
4C1F 3AB541' 1020 1374      LD   A,(HT19+1) ;REPEAT OD S/C
4C22 91      1021 1375      SUB  C
4C23 2805    1022 1376      JR   2,BCK036-4 ;OK IF AGREE
4C25'3EB2    1023 1377 BCK037 LD  A,130
4C27 C36A4B' 1024 1378      JP   HTDFMT.      ;DUD AND RESEND
4C2A'        1025 1379 BCK036 JNCW NGHIN
4C2A E5      1 1380      PUSH HL
4C2B 2A5F41' 2 1381      LD   HL,(NGHIN)
4C2E 23      3 1382      JNC  HL
4C2F 225F41' 4 1383      LD   (NGHIN),HL
4C32 E1      5 1384      POP  HL
4C33 79      1026 1386      LD   A,C      ;S/C NO TO RESET
4C34 F5      1027 1387      PUSH AF      ;NEEDED LATER !!!!!
4C35 110060  1028 1388      LD   DE,TRANS
4C38 2A1B41' 1029 1389      LD   HL,(LSTRND)
4C3B 29      1030 1390      ADD  HL,HL
4C3C 29      1031 1391      ADD  HL,HL
4C3D 29      1032 1392      ADD  HL,HL
; HL NOW HAS ADDRESS OF TRANS SLOT
4C3E 77      1034 1394      LD   (HL),A
4C3F 23      1035 1395      INC  HL
4C40 F3      1036 1396      DI
4C41 3A1641' 1037 1397      LD   A,(CLOCK+1)
4C44 E603    1038 1398      AND  3
4C46 77      1039 1399      LD   (HL),A
4C47 23      1040 1400      INC  HL
4C48 3A1741' 1041 1401      LD   A,(CLOCK+2)
4C4B 77      1042 1402      LD   (HL),A
4C4C 23      1043 1403      INC  HL
4C4D 3A1841' 1044 1404      LD   A,(CLOCK+3)
4C50 77      1045 1405      LD   (HL),A
4C51 23      1046 1406      INC  HL
4C52 EB      1047 1407      EX  DE,HL
4C53 218441' 1048 1408      LD   HL,HT1HD      ;SIMULATED DATA
4C5A 010400  1049 1409      LD   BC,4
4C59 EB00    1050 1410      LDIR
4C5B        1051 1411      INCV LSTRND
4C5B E5      1 1412      PUSH HL
4C5C 2A1B41' 2 1413      LD   HL,(LSTRND)

```

```

4C5F 23      3 1414      INC HL
4C60 224B41' 4 1415      LD (LSTFND),HL
4C63 E1      5 1416      PDP HL
4C64      1052 1418      DECM MLEF1
4C64 E5      1 1419      PUSH HL
4C65 2A4D41' 2 1420      LD HL,(MLEFT)
4C68 2B      3 1421      DEC HL
4C69 224D41' 4 1422      LD (MLEFT),HL
4C6C E1      5 1423      PDP HL
4C6D F1      1053 1425      PDP AF ;RECOVER S/C 11111
4C6E 21005B 1054 1426      LD HL,SUBCHS ;S/C STATUS AREA
4C71 5F      1055 1427      LD E,A
4C72 1600    1056 1428      LD D,D
4C74 EB      1057 1429      EX DE,HL
4C75 29      1058 1430      ADD HL,HL
4C76 29      1059 1431      ADD HL,HL
4C77 29      1060 1432      ADD HL,HL
4C78 29      1061 1433      ADD HL,HL
4C79 87      1062 1434      OR A
4C7A EDSA    1063 1435      ADC HL,DE ;ADDR OF S/C SLOT
4C7E AF      1064 1436      XOR A
4C7D 0610    1065 1437      LD B,16
4C7F'77      1066 1438 BKS21 LD (HL),A
4C80 23      1067 1439      INC HL
4C81 10FC    1068 1440      DJNZ BKS21-8 ;ZERO S/C SLOT
4C83 FB      1069 1441      EI
4C84 C3644D' 1070 1442      JP HTOFMT ;DONE

;
- - - - - 4C87' 1072 1444 BCK035 EDU 4 ;TRANS REQUEST
4C87      1073 1445      BPT
4C87 C39E4C 1 1446      JP 1+23 ;PATCHABLE BREAKPOINT
4C8A 00000000 2 1447      DEFB 0,0,0,0,0,0,0,0,0
      00000000
      0000
4E94 00000000 3 1448      DEFB 0,0,0,0,0,0,0,0,0
      00000000
      0000

4C9E      1074 1450      JNCW MGHIN
4C9E E5      1 1451      PUSH HL
4C9F 2A5F41' 2 1452      LD HL,(MGHIN)
4CA2 23      3 1453      INC HL
4CA3 225F41' 4 1454      LD (MGHIN),HL
4CA6 E1      5 1455      PDP HL
4CA7 2A7E41' 1075 1457      LD HL,(H111ND) ;REQUESTED TRANS
4CAA 7C      1076 1458      LD A,H
4CAB 65      1077 1459      LD H,L
4CAC 6F      1078 1460      LD L,A ;GET INTO ZBO FORM
4CAD E5      1079 1461      PUSH HL
4CAE B7      1080 1462      OR A
4CAF 110000 1081 1463      LD DE,D
4CB2 EDS2    1082 1464      SBC HL,DE
4CB4 E1      1083 1465      PDP HL
4CB5 FA8A4C' 1084 1466      JF N,BCK040
4CB8 2005    1085 1467      JB M7,BCK041-1
4CBA'3ED4    1086 1468 BCK040 LD A,4
4CBC C36A4B' 1087 1469      JP HTOFMT ;REQ FOR 0 OR -, MUST BE DUFF

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4CEB'ED5B4F41'	1089 1471 BCK041	LD DE,(1LSTEND)	
4CC3 E5	1090 1472	PUSH HL	
4CC4 B7	1091 1473	OR A	
4CC5 EB	1092 1474	EI DE,HL	;LAST IN HL,REQ IN DE
4CC6 ED52	1093 1475	SBC HL,DE	;D OR + 15 OK
4CCB E1	1094 1476	POP HL	
4CE9 FAB44C'	1095 1477	JP M,BCK040	;GO OUT IF DUFF
4CCC E5	1096 1478	PUSH HL	
4CED ED5B4F41'	1097 1479	LD DE,(HITRAN)	
4CD1 EB	1098 1480	EX DE,HL	
4CD2 B7	1099 1481	OR A	
4CD3 ED52	1100 1482	SBC HL,DE	;HL(- HITRAN-THIS
4CD5 F2DD4C'	1101 1483	JP P,OK717	
4CD8 E1	1102 1484	POP HL	
4CD9 224F41'	1103 1485	LD (HITRAN),HL	;NEW HIGHEST
4CDC E5	1104 1486	PUSH HL	
=4CDD'	1105 1487 OK717	EDU 0	
4CDD CD5E42'	1106 1488	CALL HTDF	;BUILD DEFAULT OUTBLOCK
4CE0 11CE41'	1107 1489	LD DE,CLKWK	
4CE3 214541'	1108 1490	LD HL,CLOCK	
4CE6 010400	1109 1491	LD BC,4	
4CE9 F3	1110 1492	DI	
4CEA EDB0	1111 1493	LDIR	
4CEC FB	1112 1494	EI	;SET CLOCK TO WORK AREA
4CED 110060	1113 1495	LD DE,TRANST	
4CF0 E1	1114 1496	POP HL	
4CF1 2B	1115 1497	DEC HL	
4CF2 29	1116 1498	ADD HL,HL	
4CF3 29	1117 1499	ADD HL,HL	
4CF4 29	1118 1500	ADD HL,HL	
4CF5 B7	1119 1501	OR A	
4CF6 ED5A	1120 1502	ADC HL,DE	;HL(-ADDR OF TRANSACTION SLOT
4CFB 11D241'	1121 1503	LD DE,TRANWK	
4CFB 010B00	1122 1504	LD BC,8	
4CFE EDB0	1123 1505	LDIR	;COPY TRAN TO WORKAREA
4D00 AF	1124 1506	XOR A	
4D01 32DA41'	1125 1507	LD (TRANWK),A	
4D04 3AD341'	1126 1508	LD A,(TRANWK+1)	
4D07 E603	1127 1509	AND 3	
4D09 32DB41'	1128 1510	LD (TRANWK+1),A	
4D0C 2AD441'	1129 1511	LD HL,(TRANWK+2)	
4D0F 22DC41'	1130 1512	LD (TRANWK+2),HL	;COPY TRAN TIME TO TRNTWK
4D12 219D41'	1131 1513	LD HL,HTDTIM+3	
4D15 11D141'	1132 1514	LD DE,CLKWK+3	
4D18 B7	1133 1515	OR A	
4D19 0604	1134 1516	LD B,4	
4D1B'1A	1135 1517 BCK042	LD A,(DE)	
4D1C 4F	1136 1518	LD C,A	
4D1D 7E	1137 1519	LD A,(HL)	
4D1E 99	1138 1520	SBC A,C	
4D1F 77	1139 1521	LD (HL),A	
4D20 1B	1140 1522	DEC DE	
4D21 2B	1141 1523	DEC HL	
4D22 10F7	1142 1524	DJNZ BCK042-1	;SUBTRACT CLOCK FROM HTD FLOC
		K	
4D24 219D41'	1143 1525	LD HL,HTDTIM+3	
4D27 11DD41'	1144 1526	LD DE,TRANWK+3	

0094800

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4D2A B7      1145 1527      OR  A
4D2B C604    1146 1528      LD  E,4
4D2C 1A      1147 1529 BCK043 LD  A,1GE1
4D2E 4F      1148 1530      LD  C,A
4D2F 7E      1149 1531      LD  A,(HL)
4D30 89      1150 1532      ADC  A,C
4D31 77      1151 1533      LD  (HL),A
4D32 1B      1152 1534      DEC  DE
4D33 2B      1153 1535      DEC  HL
4D34 10F7    1154 1536      DJNZ BCK043-4 ;ADD TRANS RELATIVE TIME
;NOW OUTBLOCK HAS ABSOLUTE TIME OF TRANSACTION
4D36 3AD211'  1156 1538      LD  A,(TRANWK)
4D39 329941'  1157 1539      LD  (HTODID+1),A
4D3C AF      1158 1540      XOR  A
4D3D 329B41'  1159 1541      LD  (HTODID),A ;COPY DID #
4D40 11A441'  1160 1542      LD  DE,HTODMS1
4D43 21D241'  1161 1543      LD  HL,TRANWK
4D46 010800   1162 1544      LD  BC,B
4D49 EDB0     1163 1545      LD1R ;COPY ENTIRE SLOT
4D4B 21D341'  1164 1546      LD  HL,TRANWK+1
4D4E AF      1165 1547      XOR  A
4D4F CB6E     1166 1548      BIT  5,(HL)
4D51 2B02     1167 1549      JR   2,BCK044-4
4D53 CBDF     1168 1550      SET  3,A
4D55 CB66     1169 1551 BCK044 BIT  4,(HL)
4D57 2B02     1170 1552      JR   2,BCK045-4
4D59 CBE7     1171 1553      SET  4,A
4D5B 32AD41'  1172 1554 BCK045 LD  (HTOERC+1),A ;STORE ERROR CODE
4D5E CD4C42'  1173 1555      CALL HTDC5K
4D61 C3934B'  1174 1556      JP   SEND ;TRANSMIT IT !

```

```

;
=4D64' 1177 1559 BCK027 EBU 8 ;NOW PERFORM DIAGNOSTIC LOGOUT
T
4D64      1178 1560      EPT
4D64 C37B4D   1 1561      JP  4+23 ;PATCHABLE BREAKPOINT
4D67 00000000 2 1562      DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
4D71 00000000 3 1563      DEFB 0,0,0,0,0,0,0,0,0
00000000
0000
4D7B DB52     1179 1565      JK  A,(F101+2) ;SWITCHES
4D7D FEFF     1180 1566      CP  OFFB
4E7F 2B0A     1181 1567      JR   2,PDI-4
4181 210641   1182 1568      LD  HL,VAPST
4C84 6F      1183 1569      LD  L,A
4E85 7E      1184 1570      LD  A,(HL)
4E86 D350     1185 1571      OUT  IP1D11,A
;
4D8B C3004B'  1187 1573      JP  PCLEND ;ROUND LOOP AGAIN
;
4D8B'F5      1189 1575 DDI  .PUSH AF
4D8C C5      1190 1576      .PUSH BC
4D8D D5      1191 1577      .PUSH DE
4D8E E5      1192 1578      .PUSH HL
4D8F DDE5     1193 1579      .PUSH IX

```

4D91 FDES	1194 1580	PUSH IV	
4D93 215ASA	1195 1581	LD HL,5A5AH	
4D96 E5	1196 1582	PUSH HL	
4D97 C300E0	1197 1583	JP 0E000H	;>>>>DDT
4D9A	1198 1584	END	

ACKD , 4144 148 106111871251
 BEK002 * 4E4E E75 E73
 BEK003 * 4E50 E79 E77
 BEK004 * 4E5A E83 E81
 BEK005 * 4E64 E87 E85
 BEK006 * 4E79 902 906
 BEK007 * 4E7E 905 903
 BEK008 * 4E8B 912 910
 BEK009 * 4E9B 919 915
 BEK010 * 4BA3 925 921
 BEK011 * 4BAE 931 927
 BEK012 * 4BB9 937 933
 BEK013 * 4BCB 945 943
 BEK014 * 4BE8 959 951
 BEK015 * 4BD2 948 960
 BEK016 * 497A 1035 967
 BEK017 * 498A 1047 977 990 993 1009
 BEK018 * 491A 985 983
 BEK019 * 4914 982 985
 BEK020 * 49B3 1065 1038
 BEK021 * 49DA 1080 1076 1078
 BEK022 * 4A4B 1140 1114 1117 1133
 BEK023 * 4A43 1134 1120 1123 1126
 BEK024 * 4ADE 1219 1190
 BEK025 * 4AE7 1226 1207 1209 1218
 BEK026 * 4B1B 1249 1247
 BEK027 * 4D64 1559 1275 1339 1442
 BEK028 * 4D5E 1281 1286
 BEK029 * 4B6B 1289 1283
 BEK030 * 4BDA 1341 1287
 BEK031 * 4BB7 1321 1314
 BEK032 * 4C0B 1364 1344
 BEK033 * 4C03 1361 1349 1354
 BEK034 * 4C17 1370 1365
 BEK035 * 4C87 1444 1367
 BEK036 * 4C2A 1379 1376
 BEK037 * 4C25 1377 1372
 BEK040 * 4CBA 1468 1466 1477
 BEK041 * 4C8F 1471 1467
 BEK042 * 4D1B 1517 1524
 BEK043 * 4D2B 1529 1536
 BEK044 * 4D55 1551 1549
 BEK045 * 4D5B 1554 1552
 BEK046 * 4B31 1268 848
 BEK047 * 4AF9 1240 1063
 BEK6ND * 4B00 840 593 1573
 BK521 * 4C7F 1438 1440
 BD15TK * 406D 138 363 365 370
 BPT H 0113 21 420 479 542 548 557 564 579 586 841 1048 1066
 1141 1240 1268 1292 1307 1445 1560
 CELL * 4142 146 111011134 113811175 1180 1198
 CHKSN1 * 421C 271 269
 CHKSNK * 4200 254 312 1277
 CLKWK * 41CE 224 1489 1514
 CLOCK * 4145 149 597 1159 1163 1166 1397 1401 1404 1490
 COKT * 4020 91
 CSTATE * 4141 145 109811112

0094800

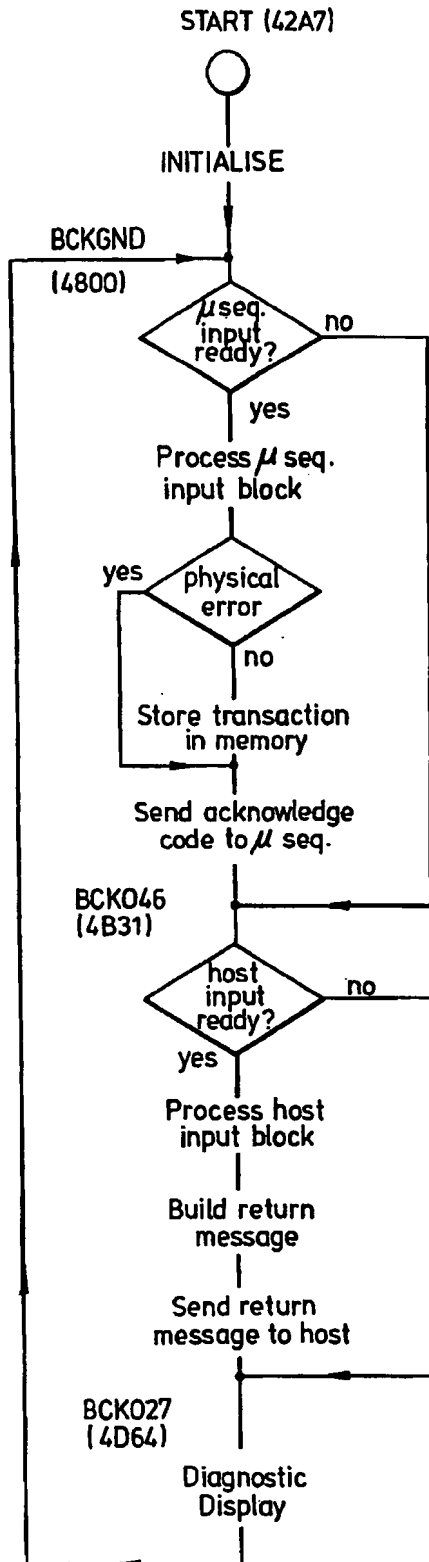
CTC	007C	45	463	464	410	414	41E
CTCVER	4020	93	401				
BBT	40E1	1575	1567				
DECV	M 1212	33	1233	141B			
ECC	423J	267	94B				
ECC1	423A	296	302				
ECC2	4242	302	300				
ENDVAR	41DE	228	363	370			
FBIT	494B	100B	10078				
FILL	M 2B10	50	360	373	386	856	1253
HITRAN	414F	154	324	1479	14B51		
HT112	418A	190					
HT113	418C	191					
HT114	418E	192					
HT15	417C	183					
HT17	4180	185					
HT18	4182	186					
HT19	4184	187	1374				
HT1BCT	4173	179	636	66B113291			
HTICK1	4190	193	1279				
HTICK2	4192	194					
HTIFL6	4172	178	625	6351	67211273	13301	
HTIHD	4186	188	140B				
HTILD	4188	189					
HTIPRT	4176	181	1370				
HTITIM	4178	182	328				
HTITND	417E	184	1457				
HTITYP	4174	180	638	1276	1342	1345	1350 1355
HTOBC1	4195	198	739	755113231			
HTOCK1	41B2	212	314				
HTOCK2	41B4	213					
HTOCSK	424C	310	1299	1555			
HTOERC	41AC	209	338	34711297115541			
HTOF	425E	319	1298	148B			
HTOF1	429B	343	345				
HTOFL6	4194	197	730	75411312	13251		
HTOFMT	4B6A	1292	1362	1369	137B	1469	
HTOHD	41AB	207					
HTOHTS	419E	202					
HTOLD	41AA	208					
HTOLTA	41AD	203					
HTOAS1	41A4	205	340	1542			
HTOAS2	41A6	206					
HTOKFS	41A2	204					
HTODID	419B	200	32211539115411				
HTORS1	41AE	210					
HTORS2	41B0	211					
HTOSER	4196	199	311	323	741	1326	
HTOTIM	419A	201	327	1513	1525		
INCK1	41BA	217	273	313	127B		
INCK2	41BC	218					
INCM	M 0117	26	617	703	765	816	849 96B 1027 1039 1053 1191 1219
			1226	1300	1332	1379	1411 1450
LDDP	M 010F	13					
LSYRND	414B	151	332	114B	122B	123011389	1413 141511471
MASK0	4059	130	947				
MASK1	405D	131					

NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
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NAME	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100
NAME	1	2	3	4	5	6																																																																																														

SIAECI ' 44L5 814 105
 SIAECI ' 41E1 219 819 8211
 SIAECI ' 44C5 892 106
 SIAETS ' 44C8 880 824 892
 SIAIBE ' 44DF 700 103
 SIAICT ' 41E0 220 705 7074
 SID ' 0060 70 487 491 495 499 502 506 510 514 518 522 526
 530 536 540 654 656 681 686 688 711 716 718
 748 1327
 SIDTB1 ' 4515 739 732
 SIDTB2 ' 452F 755 752
 SIDTB3 ' 4507 729 722
 SIDVEC ' 4028 98 497
 SLOTS ' 0000 81 119 153
 S02 ' 41E9 239 245
 SOLB ' 41DE 232 555
 S0100 ' 43C9 553
 STABLE ' 4045 123 1107
 START ' 42A7 353 89
 SUBCHA ' 4143 147 108411146
 SUBCHS ' 5800 83 : 389 391 396 1087 1426
 TERK M 2806 40 111 628 647 659 693 723 733 775 826 1315
 TOPSTK ' 4140 143 359
 TRAKEN ' BFFF 80 389 396
 TRANST ' 600B 79 1147 1388 1495
 TRANWK ' 41D2 225 1503 1508 1511 1538 1543 1546
 TRAP ' 403C 111 93 95 98 99 100 101 104
 TRNTWK ' 41DA 226 15071510151211526
 TYPE ' 4140 144 108011100 1115
 V645 ' 4B30 1266 1248
 VARST ' 4100 85 141 1568
 WAIT M 0118 5
 X1004 ' 4411 574 575
 X908 ' 43CF 555 556

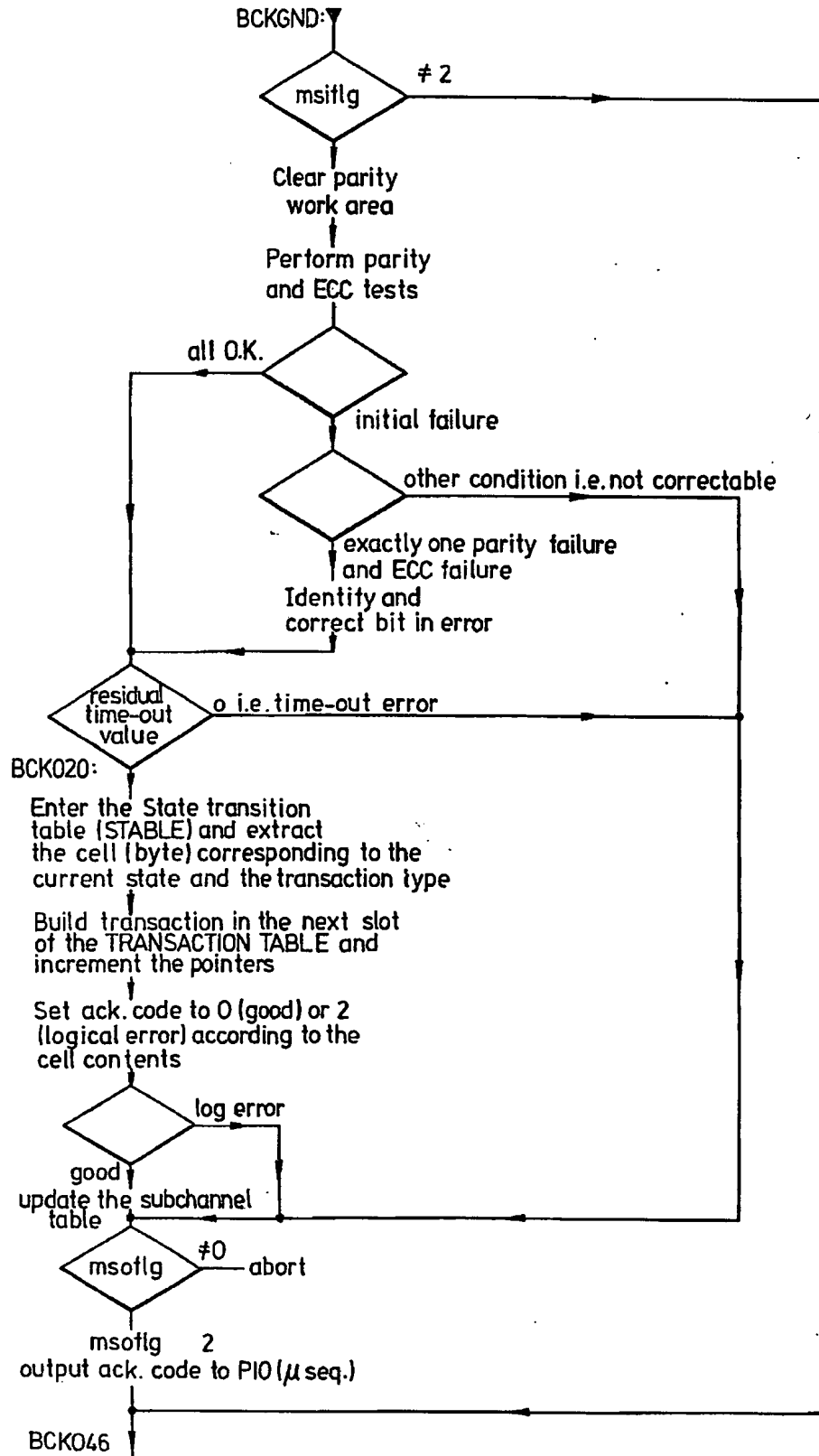
APPENDIX IV

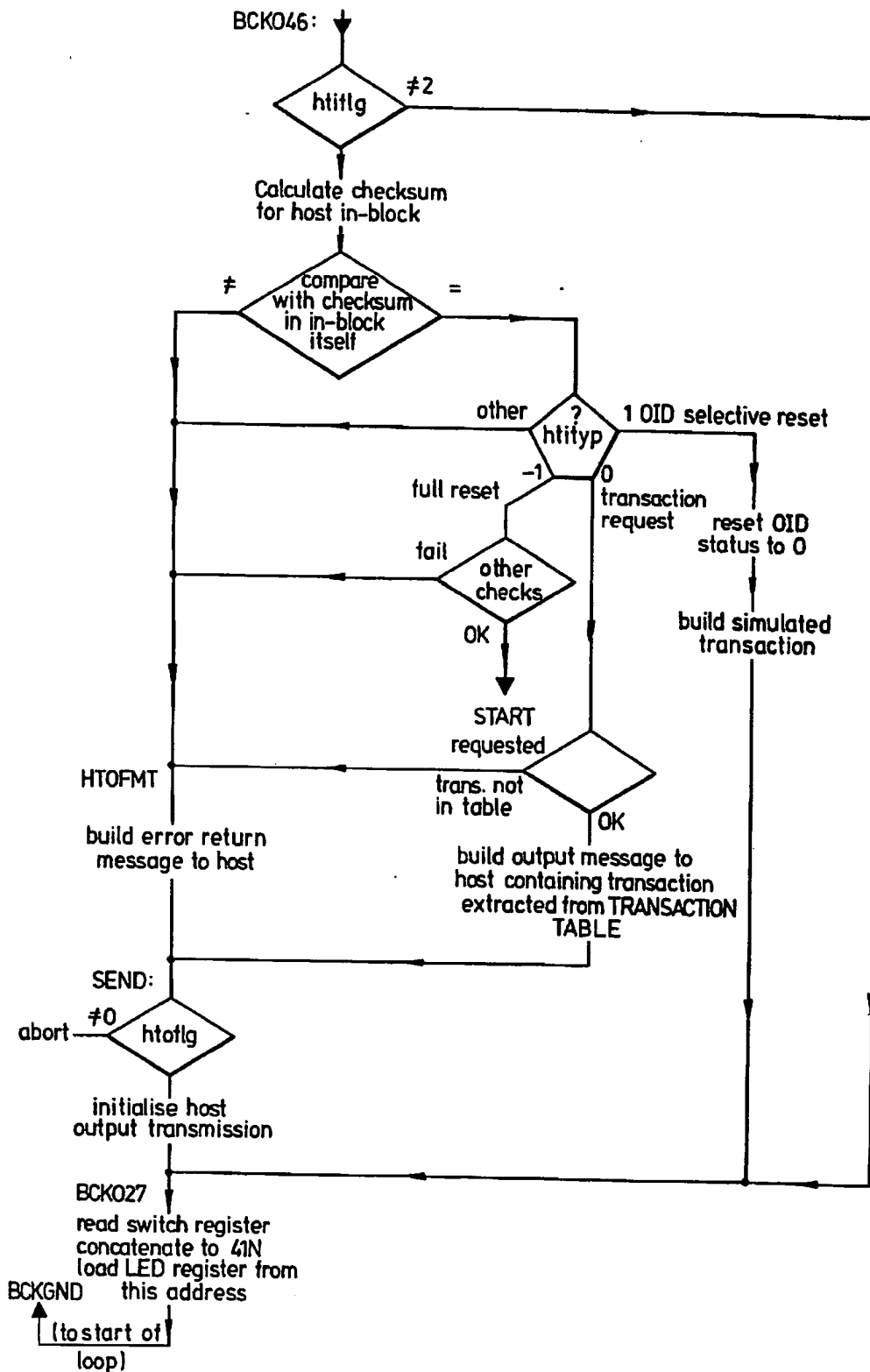
0094800



FOREGROUND ROUTINES

label	interrupt source	function
ONESEC	CTC3	one second clock
SIARCA	SIO	input on recv. char. available
(SIASRC)	SIO	error trap
SIATBE	SIO	output on xmit. buffer empty
PIAIN	PIO	input byte from sequencer
PIAOUT	PIO	output byte to sequencer

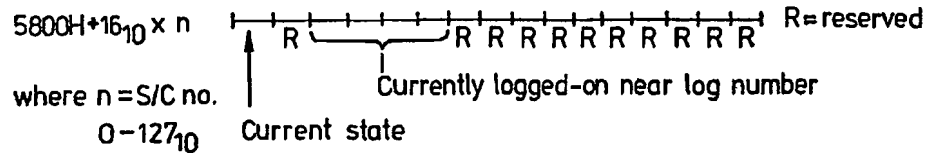




Data Formats:

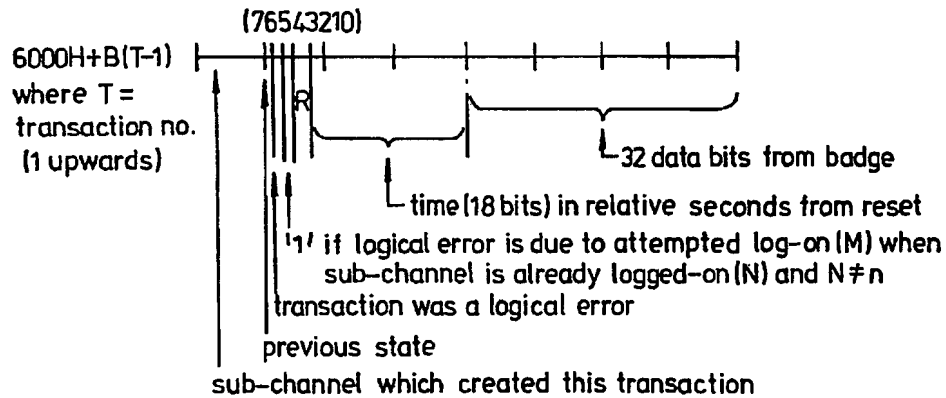
1. SUB-CHANNEL STATUS TABLE (5800H-5FFFH)

2K bytes. 128 slots of 16 bytes as follows:-

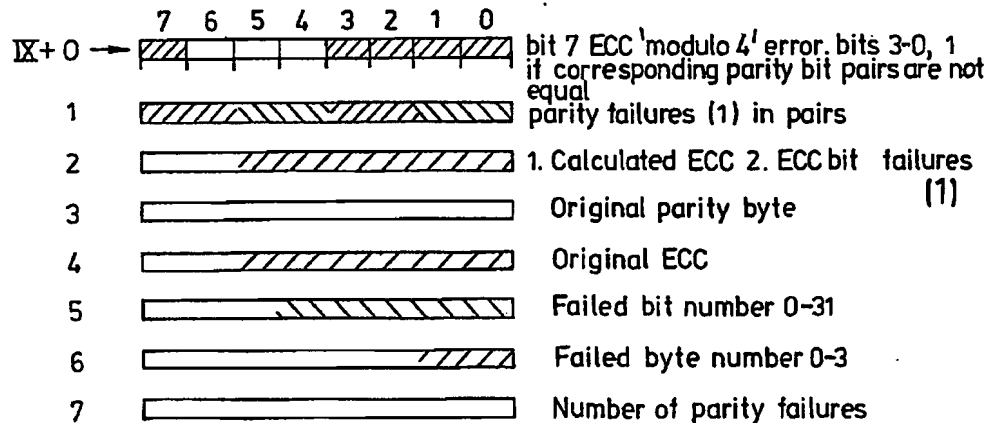


2. TRANSACTION TABLE (6000H-0BFFFH)

24K bytes. 3K slots of 8 bytes as follows



3. PARITY/ECC WORK AREA (8 bytes pointed to by IX register)



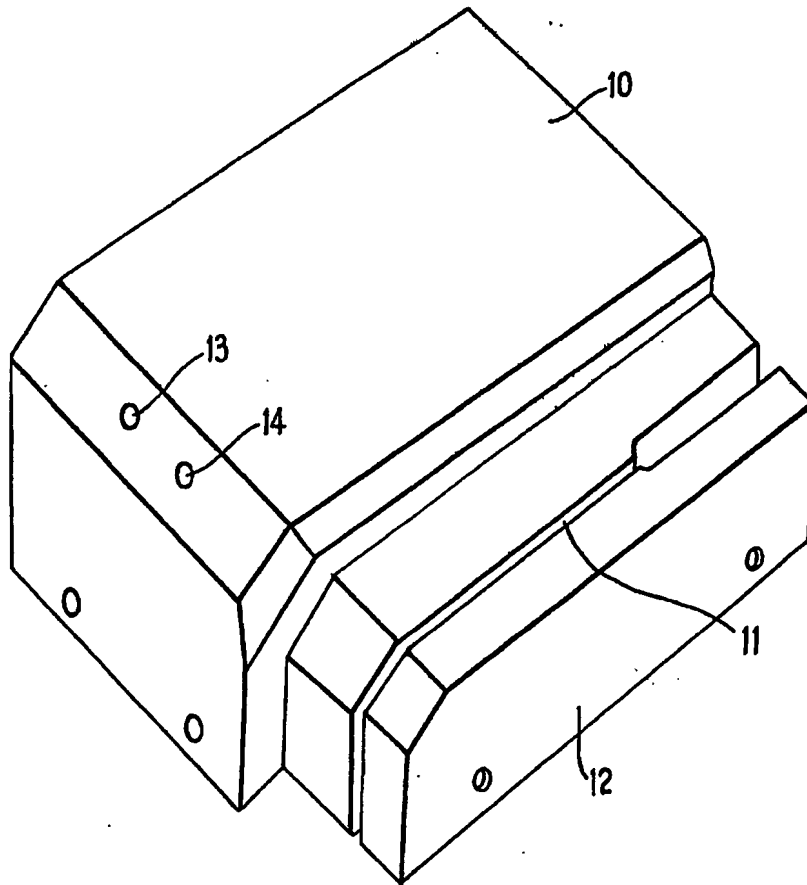


FIG.1

FIG. 2A

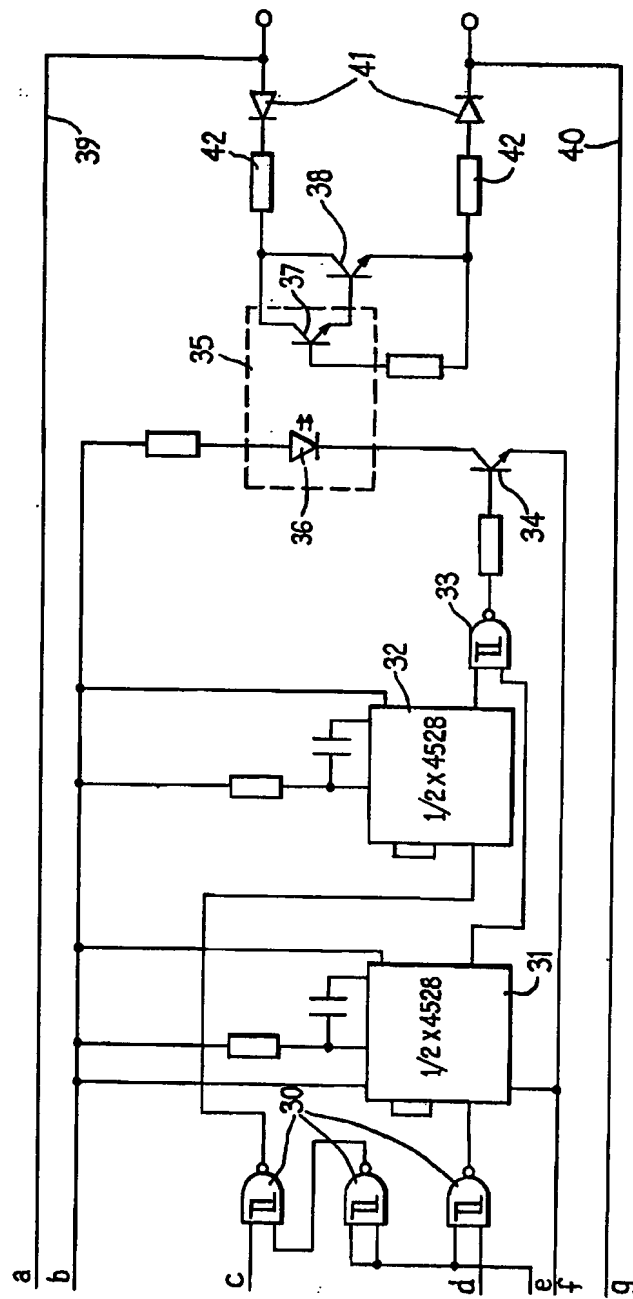
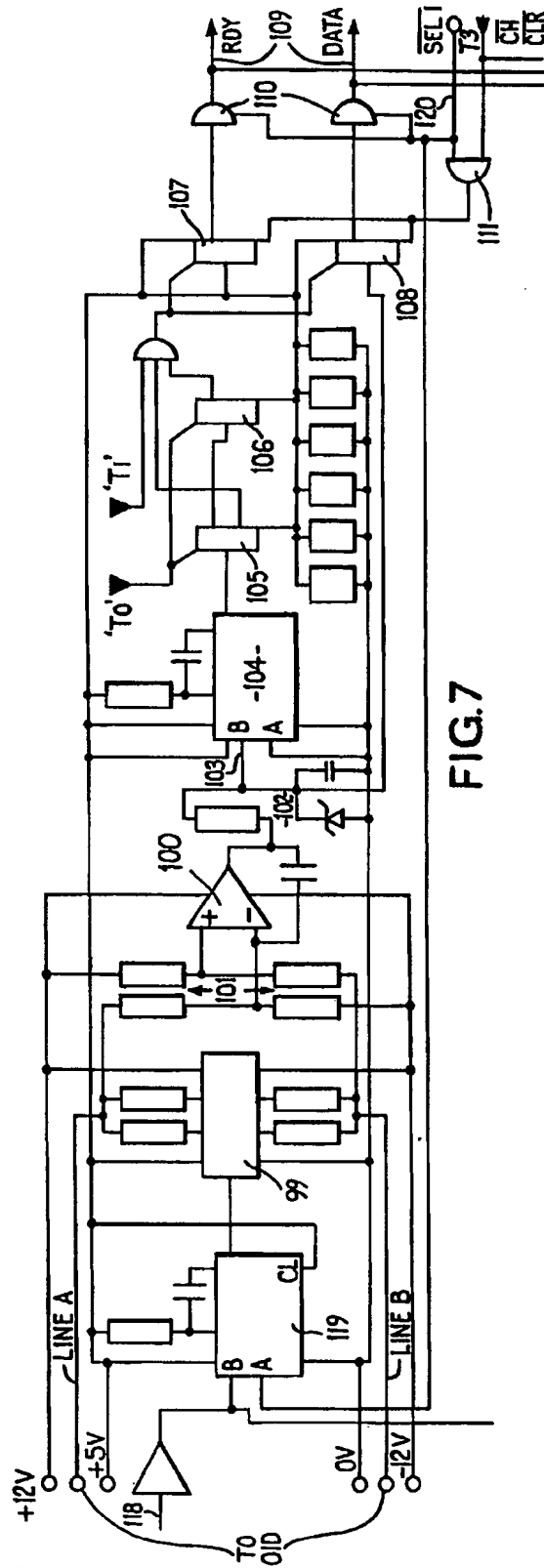
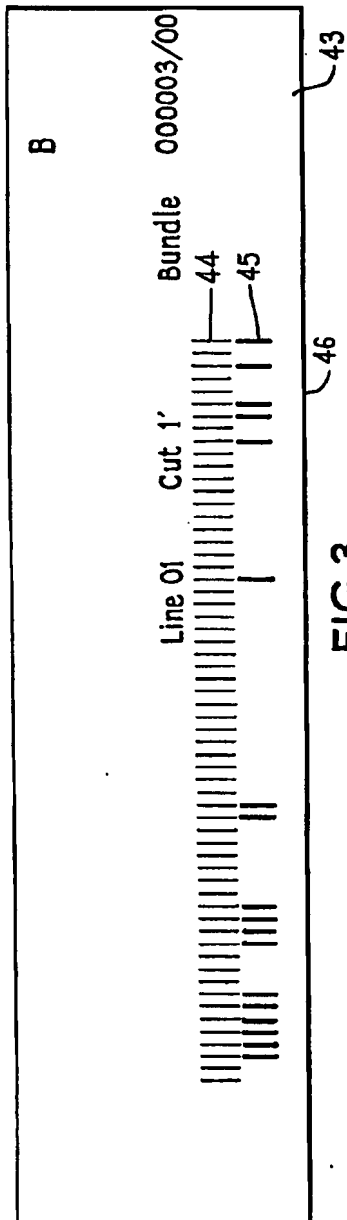


FIG. 2B



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0094800

5/15

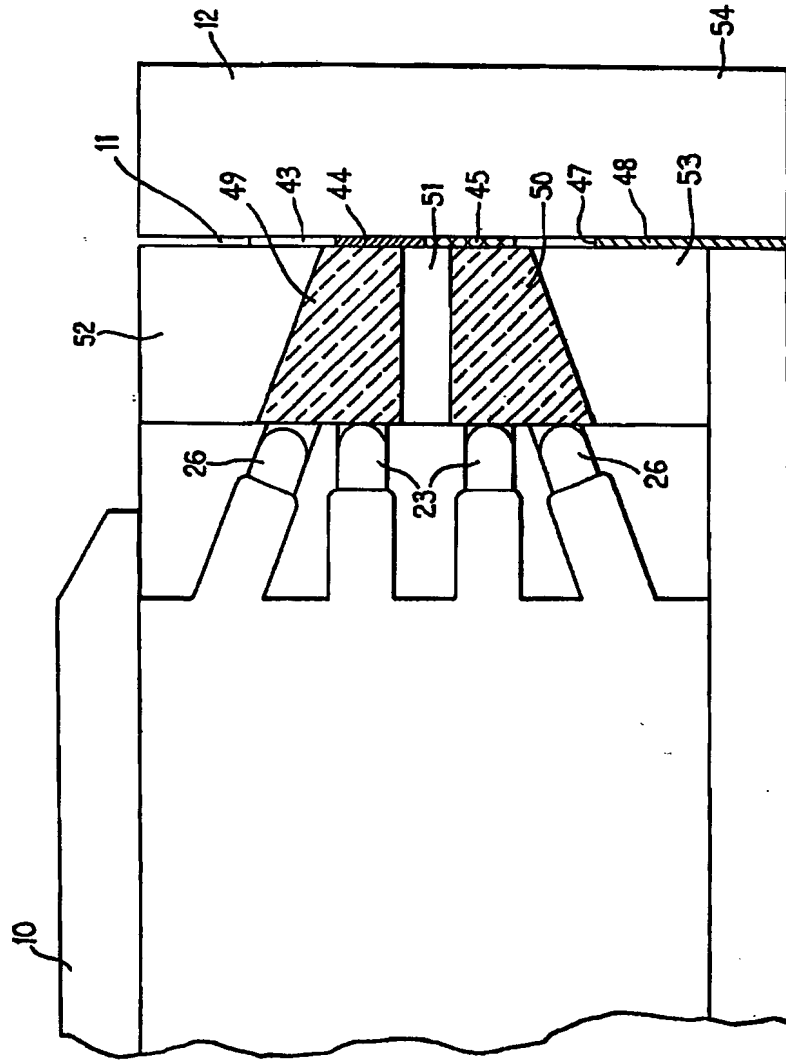


FIG.4

SECRET

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6/15

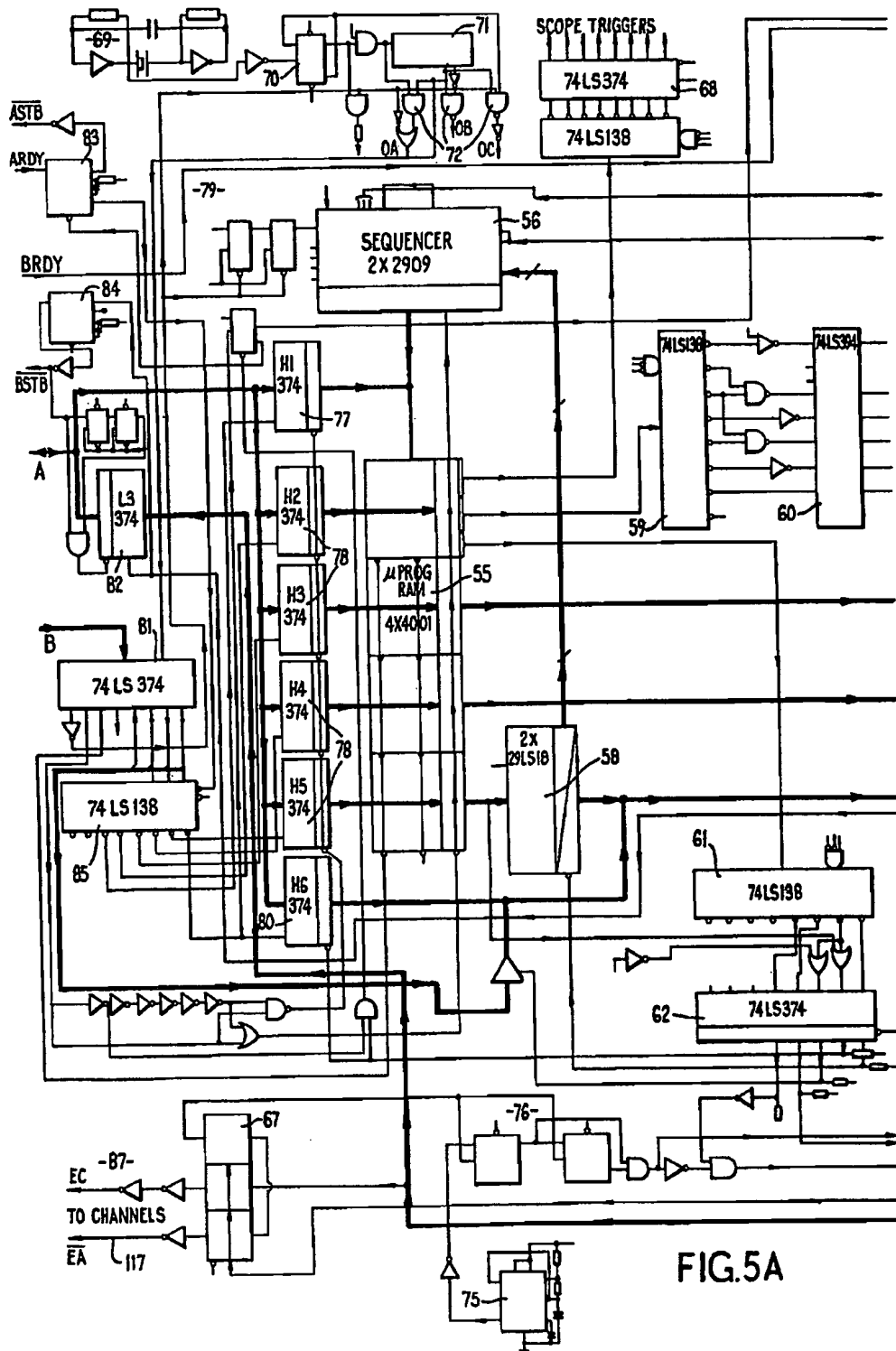


FIG. 5A

7/15

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7/15

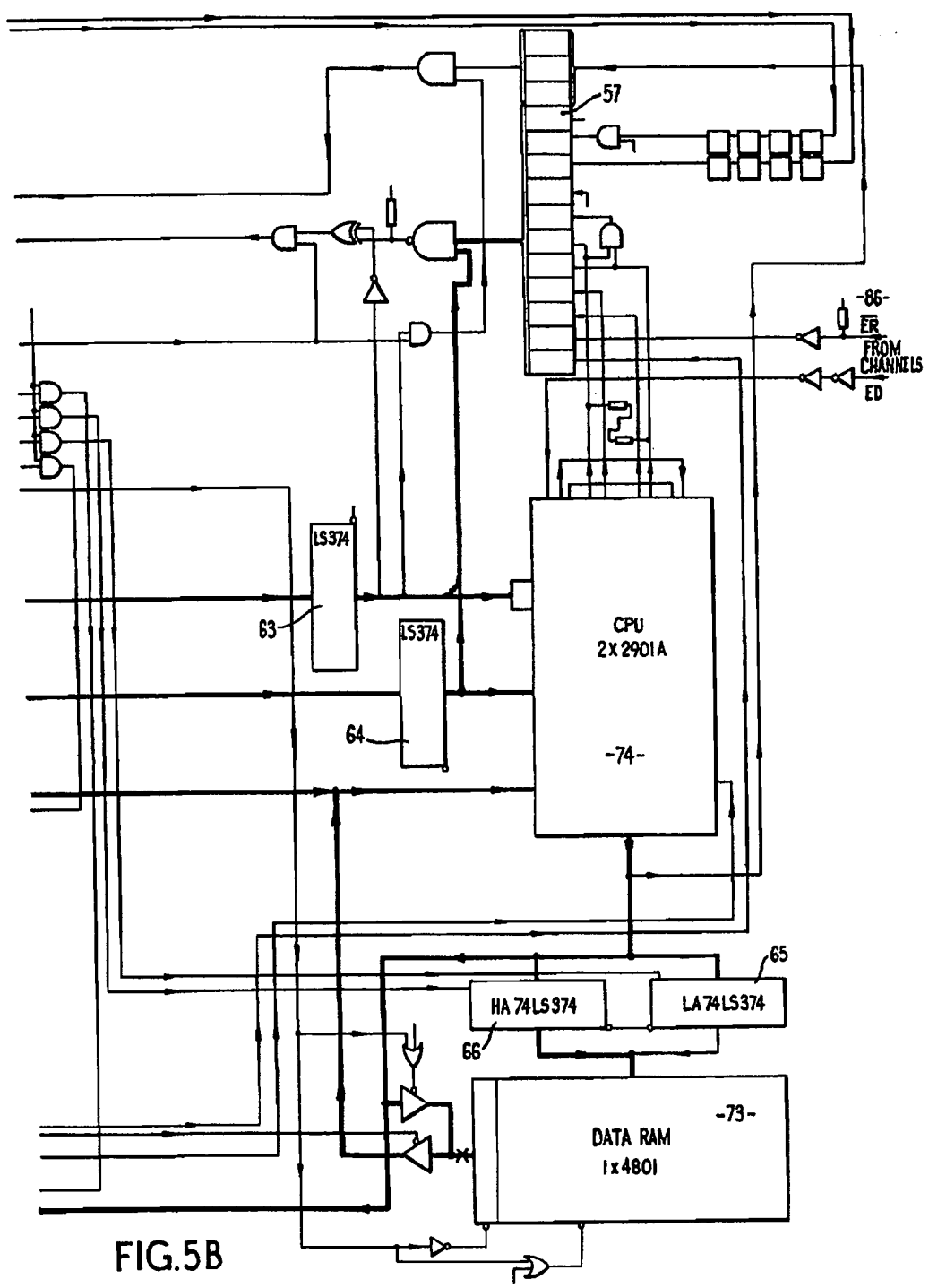
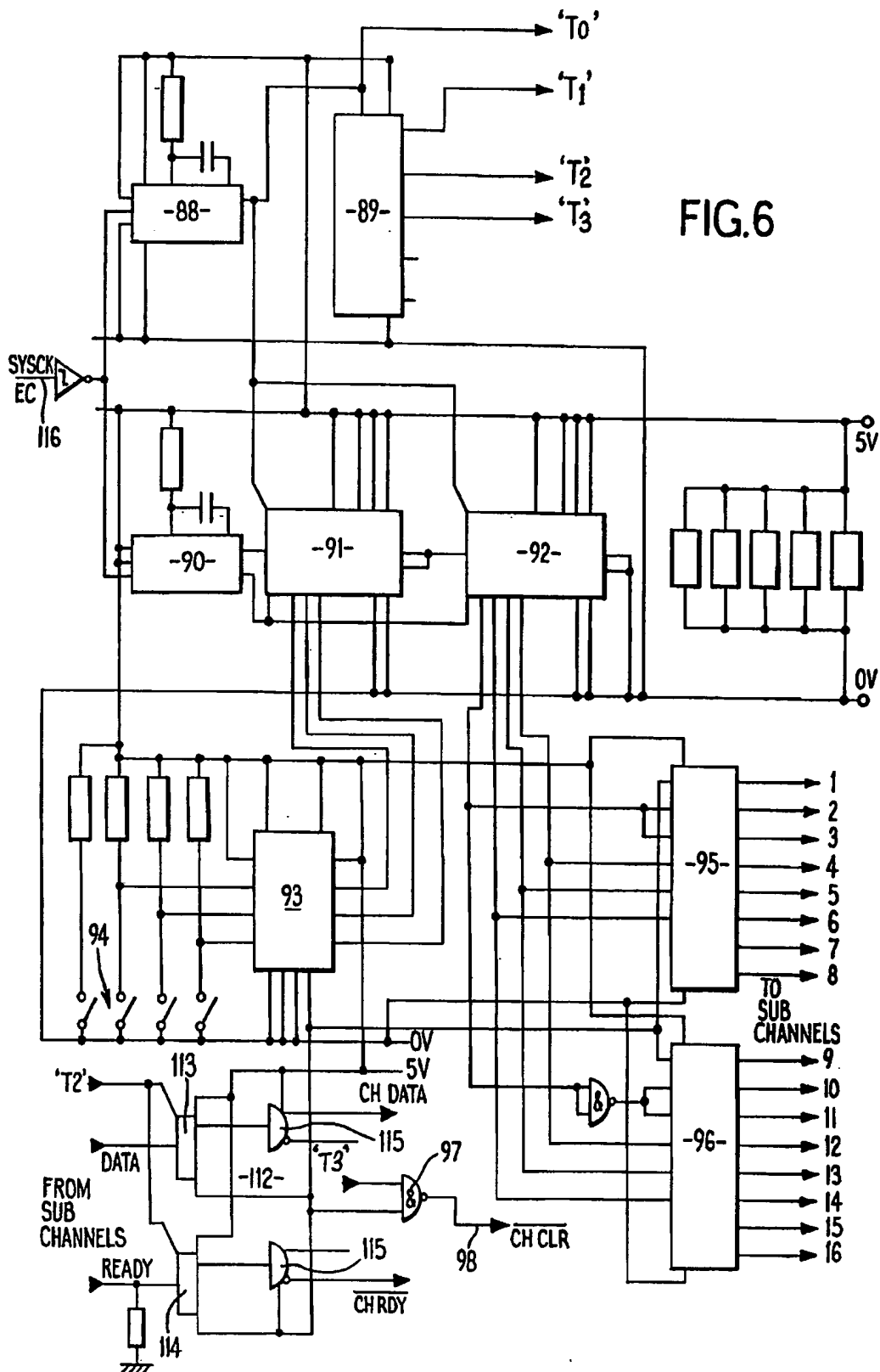
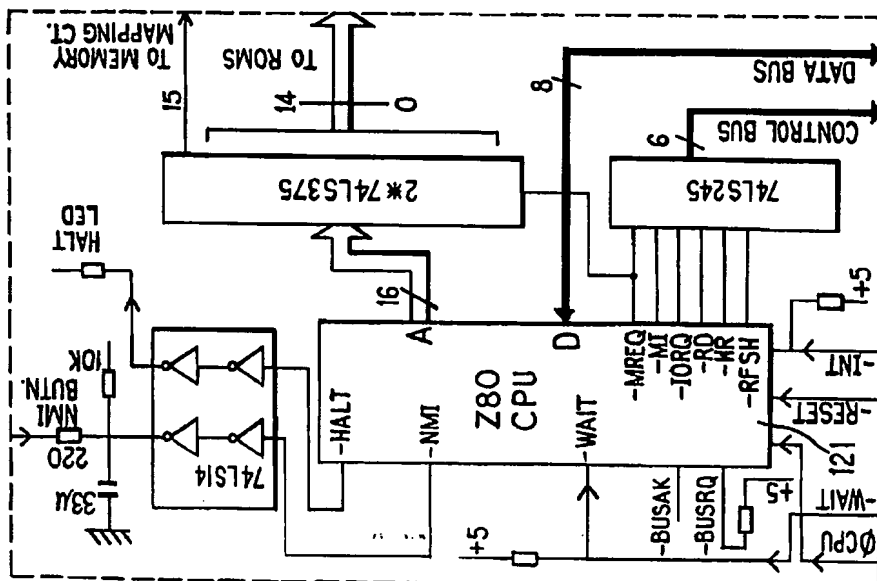


FIG.5B



[illegible]

FIG. 8A



10/15

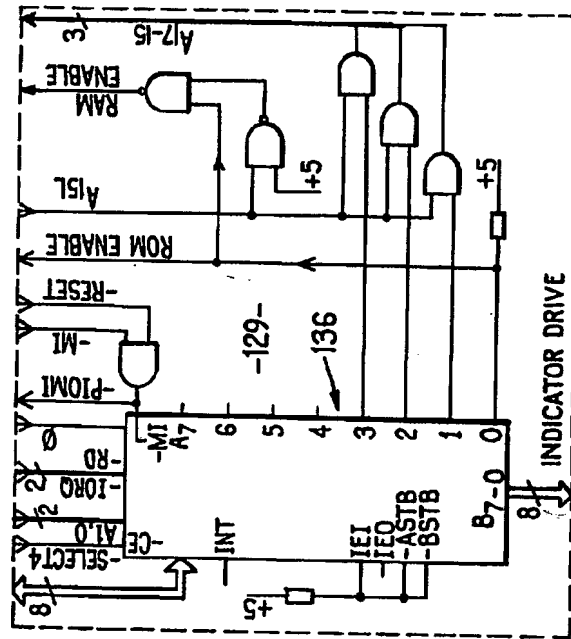


FIG. 8E

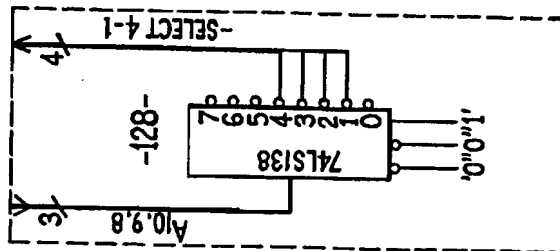


FIG. 8D

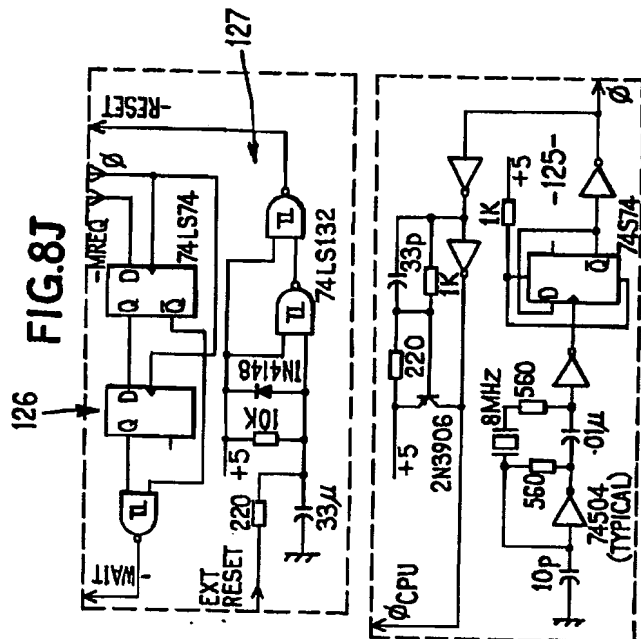


FIG. 8J

FIG. 8C

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11/15

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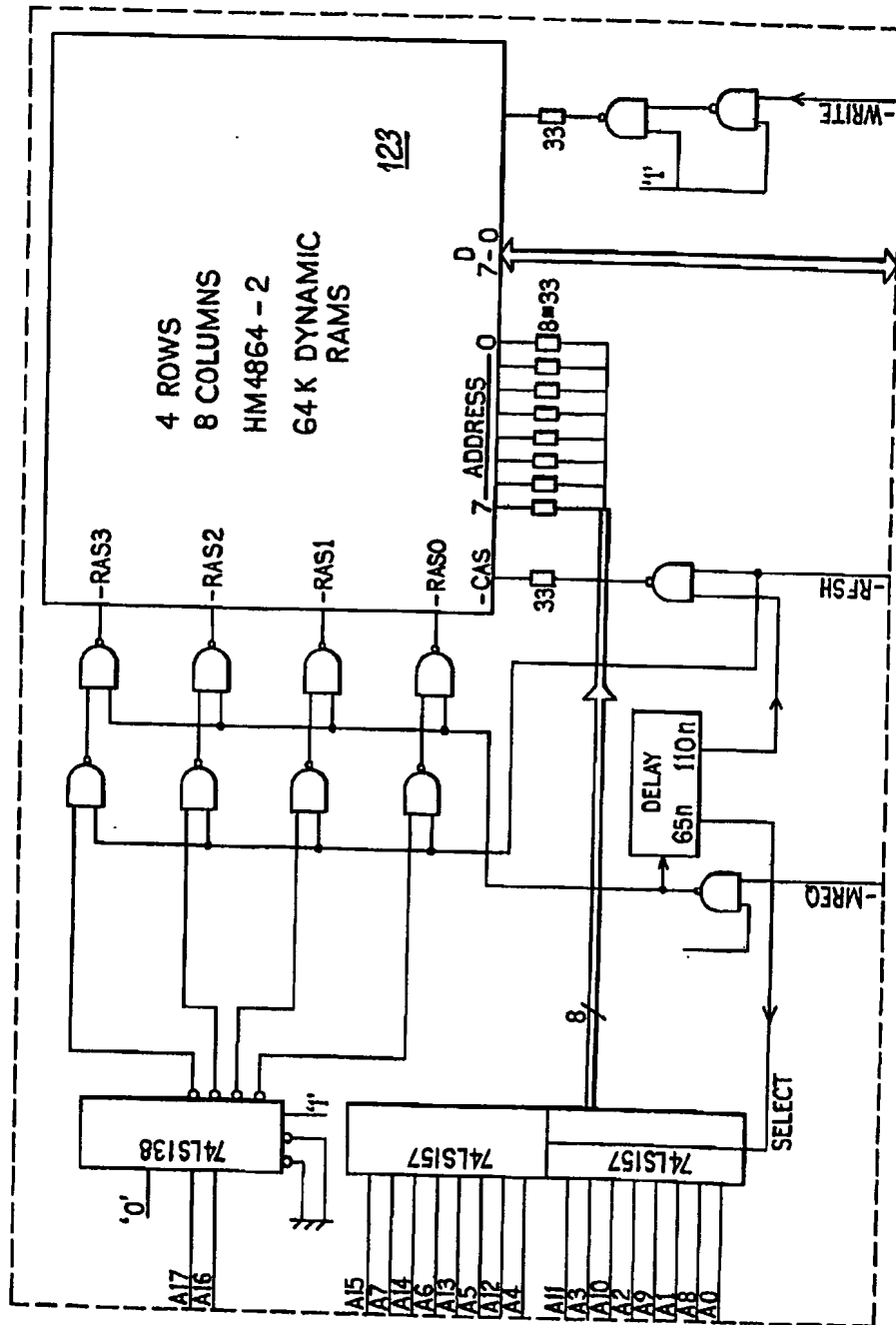


FIG.8F

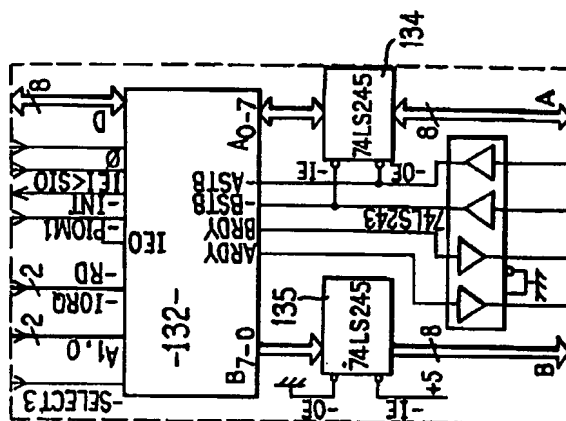


FIG. 8I

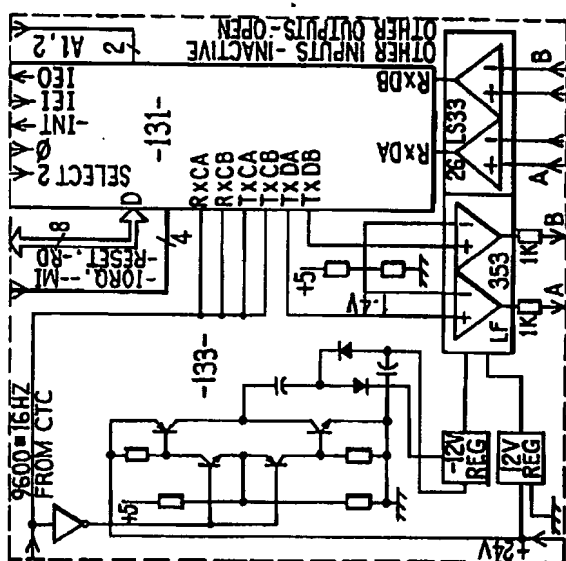


FIG. 8H

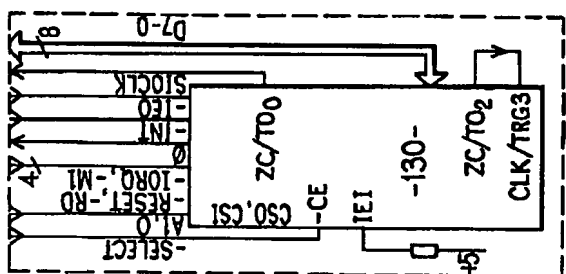
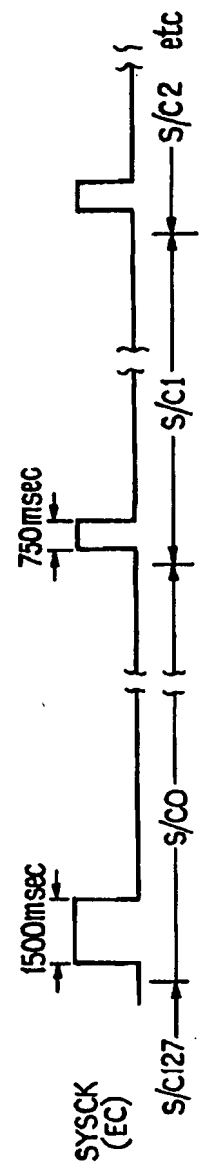


FIG. 8G



2000



* S/C PERIOD VARIES FROM 3 MICROSEC UPWARDS TO APPROX 10 MICROSEC DEPENDING ON THE MICROPROGRAM PATH

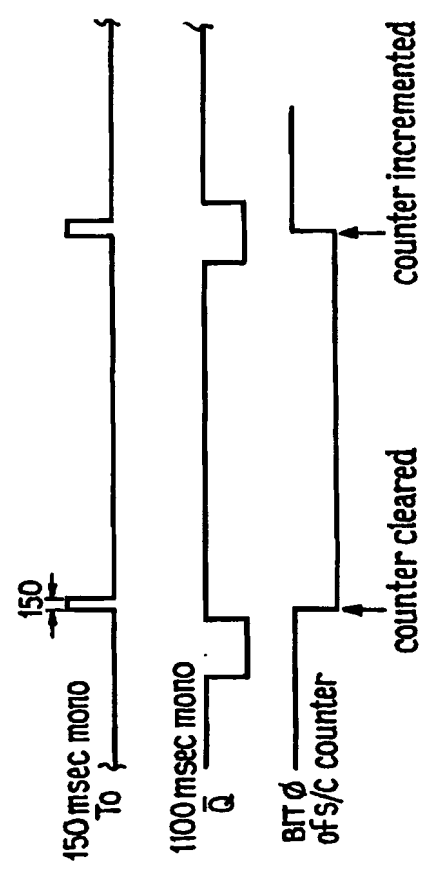


FIG.10A

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15/15

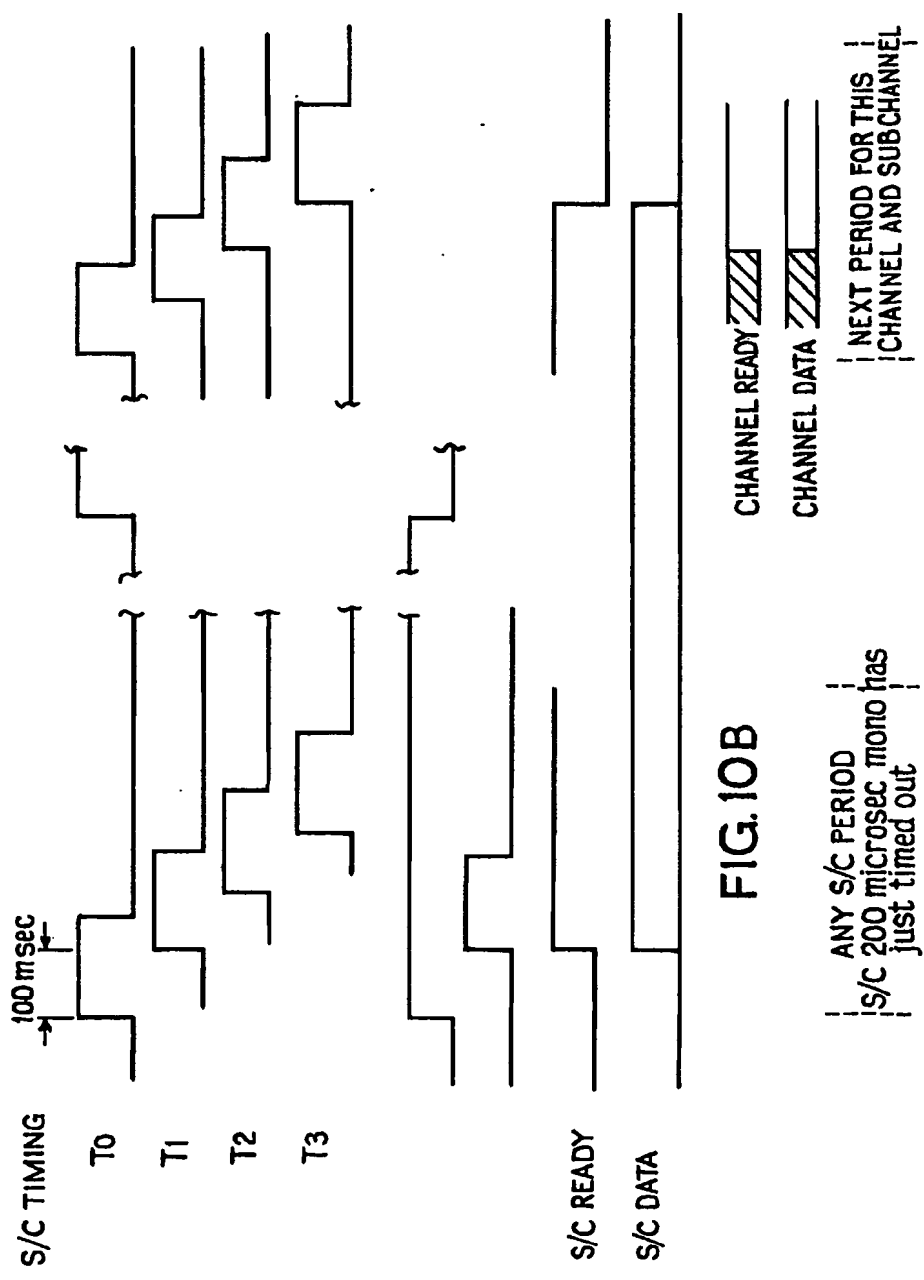


FIG. 10B